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  - Benefit of Embedded Package
  - Design Rule
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About TDK

TDK’s starting point was the first ever commercialization of ferrite.

Four great world-class innovations by TDK

Materials technology with origins in ferrite

Magnetic tape technology revolutionized music life

Fine multilayering technology promoted the miniaturization of electronic equipment

Magnetic head technology achieved awesome recording density
TDK is one of the leading electronic component manufacturers in the world.

### Passive Components
- Capacitors
- Inductors (Coils)
- EMC Components
- RF / SAW Components and Modules
- Voltage Protection Devices
- Current Protection Devices
- Temperature Protection Devices
- Sensors and Sensor Systems
- Ceramic Switching Heating, Piezo Components and Buzzers
- Transformers
- Noise Suppressing / Magnet Sheets

### Applied Magnetics Products, Applied Film Products, and Others
- Anechoic Chambers and Radio Wave Absorbers
- Power Supplies
- Magnets
- Flash Storages
- Wireless Charging
- FA Systems
- ITO Transparent Conductive Film
- Micro Modules (Substrates with Built-in ICs, Products Utilizing with SESUB)
- HDD Heads
- Lithium Polymer Batteries
TDK sales development
(Fiscals 2011 – 2015, ending March 31)

Consolidated sales:
- JPY 862.5 billion in 2011
- JPY 802.5 billion in 2012
- JPY 841.8 billion in 2013
- JPY 984.5 billion in 2014
- JPY 1,082.6 billion in 2015

Sales by product groups:
- 14% Film Application Products
  - JPY 151.3 billion
- 34% Magnetic Application Products
  - JPY 369.2 billion
- 50% Passive Components
  - JPY 541.2 billion
- 2% Others
  - JPY 20.9 billion

(Fiscals 2011 – 2015, ending March 31)
Worldwide manufacturing and R&D

Number of Employees: 88,076 (As of March 2015)
SESUB Technology

- Key Features of SESUB
- Benefit of Embedded Package
- SESUB Process Flow
- Design Rule
- SESUB application examples
**SESUB**

**SESUB = Semiconductor Embedded in SUBstrate**

- SESUB is TDK’s the state of the art substrate solution for SiP
- IC wafer is grinded to 50um and embedding in resin substrate and it enables total substrate thickness to be 300um
- SESUB is already proven technology by many customers and IC vendors
Key Features of SESUB

**Space Saving**
- Discrete Solution: 350mm²
- SESUB Module: 121mm²
- -65% reduction

**Low Profile**
- 4Layer, Substrate thickness: 300um

**Better Heat Dissipating**
- PKG Surface: 54 °C
- Junction: 63 °C
- -9°C

**Low Noise Emission**
- 35 mm
- 42 mm
- Signal line
Key Features of SESUB

Example of Space Saving

<table>
<thead>
<tr>
<th>Discrete WLCSP Solution</th>
<th>SESUB solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.0x6.4mm</td>
<td>5.0x5.0mm</td>
</tr>
<tr>
<td></td>
<td>= 45.0mm²</td>
</tr>
<tr>
<td></td>
<td>= 25.0mm²</td>
</tr>
</tbody>
</table>

Embedding IC saves PCB area almost half size compare to discrete solution.

Space Saving = 20mm² (Compare with Discrete WLCSP solution)
IC surface in SESUB is closer to a Main board with metal rich condition. This makes a heat resistance of this structure getting smaller and contribute for better heat dissipation.
**Key Features of SESUB**

**Example of Low Noise Emission**

<table>
<thead>
<tr>
<th>Conventional SiP</th>
<th>SESUB solution</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Interconnection between buried ICs by shorter signal lines within SESUB allows to improve parasitic capacitance and resistance.
Benefit of Embedded Package
Self Shielding

Discrete Solution

- Need long distance to connect btw IC and passives
- Limits area reduction
- Switcher noise on return path of PGND may couple to next signal line or emitting from this pattern itself
- Sometimes this cause EMC issue

3D Trace Pattern Routing in SESUB

- Connection among IC and passives can be concluded within the module
- PGND plane can be isolated from other GND plane
- Switching energy can be routed in internal PGND return path
- Switcher noise may be suppressed by the effect of PGND isolation

SESUB would improve noise issue due to Power GND can be isolated within SESUB
Benefit of Embedded Package
Self Shielding Effect

Discrete Solution

SESUB Solution

Optimizing of switching loop (LC loop) by SESUB contributes suppressing of noise radiation

Cin = 2.2uF (1005)
Cout = 4.7uF (1005)
Ind = 0.82uH (2012)
### Benefit of Embedded Package

**Smaller size and more I/O available**

<table>
<thead>
<tr>
<th>Example of BLE IC</th>
<th>WLCSP</th>
<th>QFN40</th>
</tr>
</thead>
<tbody>
<tr>
<td>Using same die for both WLCSP and QFN package</td>
<td>![WLCSP Diagram]</td>
<td>![QFN40 Diagram]</td>
</tr>
<tr>
<td>Number of Pin</td>
<td>34</td>
<td>40+GND</td>
</tr>
<tr>
<td>Number of GPIO pin</td>
<td>12</td>
<td>22</td>
</tr>
</tbody>
</table>

#### Discrete WLCSP Solution

- **Size**: 5.0 x 4.0 mm = 20 mm²
- Smallest possible size is 5.0 x 4.0 mm
- Number of GPIO is 12 (Maximum)
- Because of WLCSP’s GPIO

#### SESUB Solution

- **Size**: 3.5 x 3.5 mm = 12.3 mm²
- 18 GPIO Available
- User pad: 0.5mm pitch
- 7x7 matrix
- 36 pins

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**Example of BLE IC**

WLCSP

Using same die for both WLCSP and QFN package

<table>
<thead>
<tr>
<th>Number of Pin</th>
<th>34</th>
<th>40+GND</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of GPIO pin</td>
<td>12</td>
<td>22</td>
</tr>
</tbody>
</table>

**Benefit of Embedded Package**

Smaller size and more I/O available
Benefit of Embedded Package
Can be Utilize unique technology of SESUB

Flexible IC pad design
Optimizing for better heat releasing

For obtaining same current flow capacity

Free access to IC pad positions within the die makes die size optimized

Standard multi-VIA holes consume more space on IC pad

SESUB can combine multi-VIA holes into one big hole and contribute saving of IC pad space

Gaps between multiple Via holes required.

SESUB Copper Layer

IC Pad

Maximum number die embedded
In MP : 2dies
In Development : 3dies

SESUB Package for Time in Market before making SoC

0.4mm

Gap between dies : <500um

SESUB enables new function IC in time to the market

SESUB Features can be used for Next Gen Package Solution
Benefit of Embedded Package
IC direct connection

Wire Bonding: Peripheral Pad Arrangement

CSP: BGA Pad Arrangement Utilizing Redistribution Layer

Direct Connection: Formed Pad on the Elements

- No need for redistribution layer: shorter lead times, high-speed, lower-cost,
- Chip area reduction: miniaturization at lower cost
- Performance improvement for RF and BB and high-speed memory applications
- Thinner IC leads to low warpage
Complete Solution Provider

Long experience and Know how in Module Business

Design Tools → Processes → Passives → Test equip. → Sales & logistic channels WW

Design → IC Preparation → Embedding → Assembly → Tests

ICs → Other comp. → Test proced.
SESUB Development & Production Locations

- **TDK-EPC (EPCOS)**
  - Marketing, Application Design
  - (Munich, Germany)

- **TDK-EPC**
  - Assembly, Test
  - (Wuxi, China)

- **TDK**
  - SESUB Production, Process Development
  - (Kofu, Japan)

- **TDK**
  - Application Design, Marketing
  - (Tokyo, Japan)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pad location</td>
<td>Shingle side</td>
<td>Both side</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BPIC</td>
<td>Pad Pitch</td>
<td>120 um</td>
<td>50 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>Pad Material</td>
<td>Cu/Au</td>
<td>Cu / Au / Al</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Occupation ratio</td>
<td>15 ~ 60 %</td>
<td>~ 70 %</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2/S2</td>
<td>Line and space</td>
<td>34/ 46 um</td>
<td>20/ 30 um</td>
<td>10/ 20um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>Via capture/landing pad</td>
<td>150 - 250 um</td>
<td>150 - 200 um</td>
<td>Outer:110/Inner:160um</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bump capture pad</td>
<td>80 um</td>
<td>30um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IC connection Diameter</td>
<td>Unlimited max</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Heat disipation</td>
<td>Thin resin</td>
<td>Direct thermal via on IC back side</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi layer</td>
<td>4 Layer</td>
<td>2 / 4 Layer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>Pad finishing</td>
<td>Cu-OSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Encapsulation</td>
<td>Metal cap</td>
<td>or Mold</td>
<td>or Mold &amp; Shield</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SESUB Application in the Market
**SESUB Module Applications**

**Power Supply Solutions**

**POL uDCDC Buck Converter**
- Part Number: uDCDC-2923-182A
- Output Voltage: 1.82V
- Size: 2.9 x 2.3 x 1.0 mm

**Power Management Unit**
- Size: 11.0 x 11.0 x 1.6 mm

**Li+ Battery Charger**
- Part Number: SESUB-CHG-Q1350
- Size: 5.0 x 5.0 x 1.2 mm

**Complimentary Wireless Solutions**

**Bluetooth Smart (Low Energy)**
- Part Number: SESUB-PAN-T2541
- Size: 5.6 x 4.6 x 1.0 mm

**WiFi Complimentary**
- Part Number: SESUB-PAN-D14580
- Size: 3.5 x 3.5 x 1.1 mm

**2015 Aug MP Planned**

**2015 Nov MP Planned**
SESUB Module Products in the Market 1/2

**Power Management Unit**

- SESUB Module P8009

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**μDCDC Module**

- SESUB Module P8003/P8004

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**Charge Pump Module**

- SESUB Module P8008
Bluetooth Smart Module

Japanese Customer
MP: 2014/6~
Highly Integrated Power Management Unit

SESUB Solution for Mobile Application

Discrete + BGA package

18.0 x 18.0mm = 320sq.mm

-60%

11.0 x 11.0mm = 121sq.mm
Max height (inc. Shield) 1.63mm

User Pad : 0.5mm pitch,
20x21 Array, 381pads

SESUB PMU 1st Gen

10.3 x 8.9mm = 91.67sq.mm
Max height (inc. Shield) 1.43mm

-24%

User Pad : 0.4mm pitch,
21x25 Array, 415pads

SESUB PMU 2nd Gen
SESUB Solution for Wearable Application

SESUB-PAN-D14580
Bluetooth V4.1 Low Energy Module

Conventional Bluetooth Module

SESUB-PAN-D14580

Area Saving: 83%

Advantage of the module solution
- Dialog Semiconductor DA14580, Bluetooth V4.1 Smart compliant is integrated
- Tx power level: 0dBm, Rx Sensitivity level: -93dBm
- Tx current consumption: 5mA, Rx current consumption: 5mA
- Standby current: 0.8uA

Status: Sample is available, Mass Production starting from Aug 2015
**SESUB Solution for Wearable Application**

**SESUB-CHG-T24232**
Li+ Battery Charger with TI BQ24232

*excluding configuration resistors for battery charge conditions. Be flexible to various type of Li+ battery cells.*

**Advantage of SESUB-CHG-T24232**
- Saving PCB size (over 50%)
- Improving ASSY yield on application PCB
- PnP utilization for less PCB design work

**Status:** Engineering sample is available, MP start from Nov-2015
May 8th, 2015

Advanced Semiconductor Engineering, Inc. and TDK Corporation announced that both companies will enter into an agreement to establish a joint venture company to manufacture IC embedded substrates using TDK’s SESUB® technology.
Visit TDK Product Center on our web site for more detail.

Support Mail : SESUB_Support@tdk.co.jp