Expanding the Role of Fan-in and FO-WLP: Technology and Infrastructure Developments

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TRACK INNOVATION
IDENTIFY TRENDS
ANALYZE GROWTH
INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY
Mobile Products Continue to Get Thinner

Source: ASE.
iPhone Trends: Increasing Number of WLPs

Shown to scale

Source: ASE and TechSearch International, Inc., adapted from TPSS.
Drivers for WLP

• Major applications for WLP......
  – Smartphones (highest volume application)
  – Digital cameras and camcorders
  – Laptops and tablets
  – Medical
  – Automotive
  – Wearable electronics such as watch

• WLP meets system packaging needs
  – Small form factor
  – Need for low profile packages
  – Lower cost (less material)

• Form Factor is Key
  – Low profile
  – Limited space on PCB
Conventional WLP Applications

- Conventional WLPs for many device types (analog, digital, sensor, discrete)
  - Power management IC (PMIC)
  - Audio CODEC
  - RF
  - IPD, ESD protection, filter
  - LED driver
  - Electronic compass
  - Controller
  - MOSFET
  - CMOS image sensors
  - Ambient light sensors
  - EEPROM

- Conventional WLPs trends
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size Qualcomm PMIC 6.5 mm x 6.5 mm x 0.71 mm, 0.4mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch
  - Fine pitch parts need high-density PCB to route signals

Source: ASE.
Fan-In WLP Market Projections

- Conventional fan-in WLP demand
- Growth driven by greater adoption in smartphones, tablets, and wearable electronics
- CAGR of almost 9% from 2014 to 2019
Drivers for FO-WLP

- Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)
- Thinner than flip chip package (no substrate)
  - Can enable a low-profile PoP solution as large as 15mm x 15mm body
- Support increased I/O density
- Allows use of WLP with advanced semiconductor technology nodes with die shrinks
  - With increased I/O and smaller die can’t “fan-in” using conventional WLP
- Split die package or multi-die package/SiP
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance
- Improved board-level reliability
- Fine L/S (10/10µm), roadmaps for (≤5/5µm)
Multi-Die/SiP FO-WLP Solution

- 2 Layer-RDL Interconnection
- 2 Active Die + 10 Passives 0201 SMD

Source: NANIUM
FO-WLP for Automotive Application Drivers

- Growth of active safety systems for automotive applications
- FO-WLP being adopted for mmWave applications
  - Parking slot measurement (SRR)
  - Blind spot detection (SRR)
  - Adaptive cruise control (LRR 77GHz)
  - Emergency breaking
  - Lane correction
- Volumetric shrink of current and future systems (40 to 90%)
- Increased functionality with heterogeneous integration
- Improved in system performance
  - Low parasitics
  - Low inductance
- Improved board level reliability

Continent announced it is integrating Freescale’s 77GHz radar technology into its next generation short- and mid-range automotive radar modules.
Application Processor Packaging Trends

- Thinner package and smaller footprint
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- 3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out
- Silicon interposers too expensive for many mobile products
- PoP in high-end smartphones
  - Option 1: Continue with FC on thin substrate
  - Option 2: Embedded AP in bottom laminate substrate (MCP)
  - Option 3: Fan-out WLP with application processor as bottom package
  - Option 4: Some new format (SWIFT, NTI, etc.)
- FO-WLP AP in bottom PoP
  - Low profile
  - High routing density
  - Handle high power
  - System integration with competitive cost

Today’s PoP (1.0mm)

FO-WLP as Bottom PoP (<0.8mm)
• Early products included baseband processor (Infineon Wireless Division)
• Device types include RF such as Bluetooth, NFC, GPS, PMIC, automotive radar, future application processors
FO-WLP Merchant Suppliers Status

- Amkor Technology redeploying FO-WLP with new 300mm line (eWLB) in K4 plant
- ADL Engineering 200mm pilot line in Taiwan
- ASE license for Infineon’s eWLB with 300mm in Taiwan, also offers “chip last” panel version
- Deca Technologies (300mm “panel” format)
- FCI/Fujikura (embedded WLP in flex circuit)
- NANIUM (300mm wafer) license for Infineon’s eWLB
- NEPES (300mm line in Korea) based on Freescale’s RCP process
- PTI (R&D on panel)
- SPIL (300mm wafer)
- STATS ChipPAC (300mm wafer) will be purchased by JCET, license for Infineon’s eWLB
- TSMC (300mm wafer InFO WLP)
- New suppliers TBD
Industry Needs Same Package Choice from Suppliers

- **Success of McDonald’s Hamburgers**
  - Looks the same
  - Taste the same
  - No matter which geographic region

- **Packages need to**
  - Look the same
  - Have the same reliability
  - No matter which company/country location
Exceptions to the McDonald’s Hamburger Rule

• When a foundry....
  – Provides its foundry customer a packaging solution
  – Enables faster time to market with silicon and package delivery
  – Provides a warranty accepted by end customer

• When a company is vertically integrated....
  – From silicon design and fabrication to IC package and assembly to end product

• If same function is accepted
  – Different process
  – Alternative accepted with same function, performance, and reliability
Alternatives to Reconstituted Wafer FO-WLP

- Amkor’s SWIFT
- ASE’s chip last
- Conventional flip chip
- SPIL’s NTI
- Molded Interconnect Substrate (MIS)
- Embedded die solution/panel processing

Source: Amkor.

Source: Infineon.

Source: ASE.

Source: TDK.

Source: SPIL.
Amkor’s SWIFT™

- **Target Markets**
  - Mobile, Networking
  - BB, AP, Logic + Memory, Deconstructed SoC
- **Utilizes Existing Bump and Assembly Capability**
  - Polymer based
  - Flexible
    - Multi-die and large die capability
    - Large package body capability
  - Advanced die integration
    - Stepper capability down to 2um line/space
    - Die shift / orthogonal rotation elimination
    - Down to 30um in-line copper pillar pitch
  - 3D capability
    - Package stack capability using Cu pillars or TMV
ASE’s Chip’s Last Package

- **Uses low-cost coreless substrate**
  - Fine pitch capable (15 L/S today, 12µm L/S development)
  - Manufactured in double panel format
  - Assembled in strip format
  - Multi-die and passives possible
  - Can be bottom PoP

- **Thin package (<375 µm)**

- **High current and thermal handling capabilities**
  - Due to thicker Cu (15-20 µm)

- **Uses existing FC infrastructure**
  - Flip chip with Cu pillar mounted on coreless substrate
  - Mass reflow and molded underfill

Source: ASE.
Fan Out Chip Last Panel vs Wafer Utilization

Panel Size: 510x410 mm (209, 100mm²) X 2
Strip Size: 240x76.2 mm (X2L)
Strip Array: 34x13 => 442 ea

Wafer size : 300mm (70,686mm²)

6:1 Area

Source: ASE.
Molded Interconnect Substrate

- MIS-BGA offered by JCET (owns APS) and SPIL
- Versions offered by other OSATs

Source: JCET.
Is Panel Processing a Viable Alternative?

• **What size panel is feasible?**
• **Assembly of die on panel**
  - Die placement accuracy may be more difficult to control with large panels
  - Large area bonders may be required
  - Throughput (time required to pick and place die in panel)
  - How is placement accuracy impacted by tape and mold compound?
  - What level of inspection is required to verify accuracy? What speed?
• **Dielectric dispense methods?**
  - How to control run-out at edge?
  - Need inspection for even coating?
• **Molding materials and process?**
• **Panel warpage**
  - Warpage increases with panel size
  - Impact of materials (mold compound and filler)
  - What type of inspection is required and how will it work with warped panels
• **Via formation method (minimum via diameter)**
  - Via alignment
• **Metal plating**
  - Metal to dielectric interface (what inspection requirements?)
  - How to sputter seed layer?
• **Interconnect reliability? Inspection for broken metal traces etc.**
• **Singulation method?**
• **Solder ball placement and inspection method?**
Additional Considerations for Panel Processing

- **Warpage (impacts assembly/manufacturability)**
  - Heterogeneous materials and non-symmetric structures can cause bowing
  - Polymer materials with adapted CTE and modulus, plus low shrink

- **Accuracy/resolution (miniaturization)**
  - Improved optical recognition systems for placement equipment
  - Imaging with high depth of focus and high resolution

- **Yield (impacts cost)**
  - Suited materials and components
  - Optimized processes
  - Production experience

Source: Fraunhofer IZM.
Conclusions

- **Mobile products require low profile packages**
  - Fan-in WLP
  - FO-WLP

- **Demand for lower cost solutions drives adoption of new package designs and formats**
  - Round panels?
  - New chip last packages?
  - MIS on modified leadframe?
  - Large area processing?

- **Many package choices**
  - Few standard options except conventional WLP
  - Growing number of companies selecting FO-WLP with reconstituted wafer
  - Alternatives will continue to be developed
Thank you!

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