SiP Solutions for IoT / Wearables

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## Electronic Products Integration Trend

<table>
<thead>
<tr>
<th>Year</th>
<th>~2000</th>
<th>2010</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main Stream Products</strong></td>
<td>PC / Notebook</td>
<td>Mobile Phone / Tablet</td>
<td>IoT / Wearables</td>
</tr>
<tr>
<td><strong>Market Features</strong></td>
<td>Feature: Standard Platform, High Volume Customer: Brand Name OEMs</td>
<td>Feature: High Matrix, Low Volume Customer: Many new customers in various application market</td>
<td></td>
</tr>
<tr>
<td><strong>Integration Trends</strong></td>
<td>SoC / PCBA</td>
<td>SoC / SiP</td>
<td>SiP / PCBA / SoC</td>
</tr>
</tbody>
</table>
| **SiP Opportunity** | Camera, Finger Print, Wireless Connectivity | • **Sensor Related** SiP (Camera, Finger Print)  
• **Analog Based** SiP (Connectivity, Analog, PMIC, PA/LNA) | Wireless Connectivity, PMIC, Sensor |
| **Remark** | • SoC plays major role on function integration  
• SiP is only adopted in high end smart phone. | | • Modulize is a trend and SiP plays more important role in this high matrix market |
SiP Market Overview

SiP Applications:
- NB application moves in saturation stage.
- Mobile phones & Tablets is still in growing phase
- IoT & Wearables is in the beginning of growth.

Source: Gartner, Morgan Stanley, SPIL estimation
IC / SiP Design Requirement for IoT market:

1. **MCU**: Micro Controller, usually ARM base, MCU instead of AP
2. **Sensors**: Temp, Vibration, Gyroscope, Moisture, Pressure, Altitude...
3. **Power Management**: High integration on Active + Passives
4. **Memory**: Flash, NVM, SRAM
5. **Wireless, Connectivity**: WiFi, BLE

=> Low Cost + Great Performance + Low Power + Easy design-In = Low Entry Barrier
Challenge & Key Success Factors

In 2017, 50% of IoT and wearable devices will be provided from start up companies built within 3 Years

- Gartner

**IoT / Wearable Devices Market Features:**
- Non-Standard Products – customers need high integration solutions
- Various Start up Players – customers don’t have much resource on too complicated system design
- More Sensitive on Cost, Size, Power and especially “time to market”

**Key Success Factors of SiP Solutions for IoT / Wearables:**
- Provide Total Solution (IC Package + System Level Assembly)
- System Design and Testing Capability
- High integration and miniaturization solutions
  1) EMI Shielding on Package
  2) 3D / Embedded PKG Structure
  3) Antenna in Package
Total Solution: Direct Package to SiP

- Wafer Bumping
- Wafer Sort
- Module Assembly
- Chip/Package Design
- Function Test

Wafer Bumping:
- Characterization
- Reliability validation
- Footprint arrangement.
- RDL.
- Bump mask design

Chip/Package Design:
- FOC/Repsv/RDL
- WLCSP

Function Test:
- Probe card design
- Test program optimization

Module Assembly:
- System Level Design
- Schematic/layout design
- Package/process design

Drop Ship:
- Test System Setup
- Socket/change EVB design
- Test program Development

SiP Module & Package Co-Design:
- SMT
- D/W Bond
- Molding
- EMI Coating

SiP Module Design:
- SiP Module & Package Co-Design
- Function Test
- Module Assembly
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- Molding
- EMI Coating
Design Simulation for Wearables

Simulation

Thermal
- Critical Thermal
- Temperature Contour
  Flotherm
  ANSYS

Stress
- Max. Warpage
- Solder Fatigue Life
  Mold Flow
  ANSYS
  LS-DYNA

11a/b/g/n MIMO + BT4.0 SiP Module

11b/g + BT SiP Module

Electrical
- S Parameter
- Signal/Power Integrity
  EMI Simulation
    HFSS, Power SI
    HSPICE, ADS
    Q3D, TPA

EMI, Antenna

11a/b/g/n MIMO + BT4.0 SiP Module

11b/g + BT SiP Module
SiP Key Process Development

2012:
- LGA/BGA Package
- Stack Die on Passives
- Elevated Inverted F Antenna

2013:
- EMI Coating w/ Partition
- SiP w/ Embedded Inductor

2014:
- Stack Die on Passives
- Package w/ Antenna & EMI Shielding

2015:
- EMI Coating w/ Partition
- SiP w/ Embedded Die & Inductor (Under Review)

2016:
- LF EMI Solution
- Directional Antenna for NFC

EMI Coating
Embedded Solution
Antenna in Package
EMI Coating & SE Measurement / Simulation

Coating Thickness Measurement

SE (Shielding Effectiveness) Measurement Result

Frequency (Hz)

SE (dB)

LF Solution: Molding + Stack Ferrite + Metal Coating

Normal Solution: Molding + Metal Coating: SE < 10dB @ 1 < 3MHz

HF Solution: Molding + Metal Coating + Stack Ferrite + Metal Coating

SE Simulation vs. Measurement

EMI Scan
3D SiP Structure

1. Embedded Die in Substrate
   2. Work with sub. Vendor to embedded die in substrate

3. Pros:
   (1) Size & Thickness reduction
   (2) Better electrical and thermal performance

4. Cons
   (1) Higher cost
   (2) Long substrate lead time

1. Stack Die on Passives
2. The seating plane for the top die is made of various height passives with epoxy film.

3. Pros:
   (1) Size reduction
   (2) Low cost

4. Cons
   (1) Thickness
   (2) Thermal dissipation

1. Dual Side w/ Cavity Structure
2. Use 2L Interposer substrate to form cavity structure

3. Pros:
   (1) Size reduction
   (2) High component density

4. Cons
   (1) Thickness
   (2) Thermal dissipation
Stack Die on Passives

Total Height: 0.70mm

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Substrate Thickness</td>
<td>0.136mm</td>
</tr>
<tr>
<td>D</td>
<td>Die Thickness</td>
<td>125um</td>
</tr>
<tr>
<td>F1</td>
<td>Film Thickness after Die stacked</td>
<td>45um ± 10um</td>
</tr>
</tbody>
</table>
| H | Passives Thickness (01005)                           | R: 0.13 ± 0.02 mm, C or L: 0.20 ± 0.02 mm
Embedded Inductor

Original SiP Module
- Substrate: 2L
- Package Height: 1.3mm

Discrete Inductor
- Size: 2 x 1.6 x 1.0 mm
- Inductance: 1.2uH @ 2MHz, Rdc = 80 mOhm

Advantages of Embedded Inductor:
1- Package height reduction
2- Lower power consumption due to lower Rdc (P = I^2 * Rdc)
3- Lower EMI concern on PCBA/Package - as most magnetic field are trapped in toroid ferrite

Application: PMIC, DC/DC converter

Evaluation on “Embedded Inductor”
- Substrate: 2L
- Package Height: 0.9mm

Embedded Inductor (Simulation)
- Size: 2.1 x 1.5 x 0.55 mm
- Inductance: 1.4uH @ 2MHz, Rdc = 70 mOhm
# Benchmark on Antenna in Package Solutions

<table>
<thead>
<tr>
<th>Features</th>
<th>Package with Elevated Inverted-F Antenna (in package)</th>
<th>Package with Printed antenna (in substrate)</th>
<th>Package with Coated antenna (on package surface)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Antenna Performance - Efficiency, Gain, VSWR Bandwidth,</strong></td>
<td>★★★★☆</td>
<td>★★★☆☆</td>
<td>★☆☆☆☆</td>
</tr>
<tr>
<td><strong>Radiation Pattern</strong></td>
<td>★★★★☆</td>
<td>★★★☆☆</td>
<td>★☆☆☆☆</td>
</tr>
<tr>
<td><strong>Assembly Process</strong></td>
<td>★★★☆☆</td>
<td>★★★☆☆</td>
<td>★☆☆☆☆</td>
</tr>
<tr>
<td><strong>Dimension (include Keep out area)</strong></td>
<td>★★★★☆</td>
<td>★★★☆☆</td>
<td>★☆☆☆☆</td>
</tr>
</tbody>
</table>

**Remark**
- **Features**
  1. Antenna in molding Compound
  2. Method of frequency adjustment

- **Features**
  1. Multi-layer antenna to shrink size
  2. Special anti-human body design

- **Features**
  1. sputter coating on package to form antenna
  2. Thin coating layer limit performance
  3. Complicate process for signal feeding
Antenna and Package Co-Design

Information Input & Study

1. Applications
2. Package Size
3. Certification Comply
4. Assembly Structure
5. Required SPEC
   - Gain
   - Efficiency
   - Bandwidth
   - Radiation Pattern

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Antenna Package Co-design

1. Antenna Design/Simulation
2. Substrate Design
3. Total SiP Design

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Sample Build & Verification

Performance Verification/Measurement
- Gain
- Efficiency
- Bandwidth
- Radiation Pattern

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>X-Z plane (Phi=90°) (H+V: dB)</th>
<th>Y-Z plane (Phi=90°) (H+V: dB)</th>
<th>X-Y plane (Theta=90°) (H+V: dB)</th>
<th>Efficiency (H+V:%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.400</td>
<td>3 -7.5 0.6 -7.6 -10.5 -15.2 26</td>
<td>3 -7.2 0.9 -6.8 -8.3 -10.1 28</td>
<td>2.400 2.5 -7.2 0.5 -6.6 -6.1 -7.7 26</td>
<td></td>
</tr>
</tbody>
</table>

1. Package with Elevated Inverted-F Antenna
2. Features:
   (1) Size Reduction, 2.4GHz antenna in 6.5x6.5mm
   (2) High Antenna Efficiency > 30%, Gain > 1dBi
   (3) Support High Density Component in Package

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Sample Build & Verification

1. Package with Folded Antenna
2. Features:
   (1) Feasible EMI Shield & Antenna co-existence for Certification (FCC/CE)
   (2) High Antenna Efficiency > 35%
   (3) Anti-Human Body Effect

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Wi-Fi, Bluetooth, and CE compliance symbols are shown.
NFC Antenna Development

Abracon:ANFCA-1510-A02

<table>
<thead>
<tr>
<th>Item</th>
<th>Current Antenna</th>
<th>SPIL Proposal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size(mm)</td>
<td>15 x 10</td>
<td>6 x 2</td>
</tr>
<tr>
<td>Operation Freq.(MHz)</td>
<td>13.56</td>
<td>13.56</td>
</tr>
<tr>
<td>Inductance(uH)</td>
<td>1.8±10%</td>
<td>2.14</td>
</tr>
<tr>
<td>Q Factor min.</td>
<td>30</td>
<td>22.4</td>
</tr>
<tr>
<td>DCR Max.(Ω)</td>
<td>1.5</td>
<td>1.8</td>
</tr>
</tbody>
</table>

Application:
- Wearable
- Health care ID scan
- Ticketing system

Status: Target Finish Design by 2015/09, Qaul Pass by 2016/01
Example of SiP for IoT / Wearables

MCU + WiFi COB Solution
Size: 22x19mm
- Include WiFi + MCU + Memory
- Component Count: 50
- Process: wafer thinning, stack Die on FC, MUF, EMI Coating

MCU + WiFi SiP solution
Size: 10x10mm

MCU + BLE COB Solution
Size: 18x12mm
- Include BLE, EEPROM, X’tal, Antenna
- Component Count: 28
- Process: stack die on passives, Antenna in Package, Molding

MCU + BLE SiP solution
Size: 6.5x6.5mm

80% size reduction

WiFi Speaker
WiFi Plug
WiFi Sensor Hub
WiFi Bulb
WiFi Air Conditioner

BLE Door Lock
BLE Toy
Swimming Band
Hand Band

iRhytm

75% size reduction

80% size reduction

Hearing Aid
Swimming Band
Hand Band