Put the Pieces Together in the Materials Space: Advanced Materials Solutions for 10nm and Beyond

Dr. Spencer Tu, Director, Taiwan Technology Center
Increasing Interdependency Within the Semiconductor Ecosystem to Meet Performance, Yield and Cost Targets for 10nm and Beyond

Opportunity to “put the pieces together” in the materials space

- Advanced precursors, advanced surface preparation, novel doping
- Materials, handling, sensing, and delivery components
- Enabling new paradigms

Customers Care About:
- Technology Performance
- Process Yield
- Device Cost

Significant overlap within the Semiconductor Ecosystem
- Increasing need to work together in this space for advanced solution
- Targeted collaborations are key to the challenges advanced node
Increased Interaction Among Wet, Deposition, Implant, and Plating Processes When Integrating Materials

Understanding the integrated stack and material interactions enables tailored solutions that fit customer requirements.
FEOL: New Channel Materials and 3D Structures

Dimensional scaling was the main driving force of in the past 50 years.

High-K/Metal gate transistor improved performance, Intel.

FinFET and Trigate is structure renovation.

New Channel Materials
- e.g. SiGe, III-V, ...
- Need: Surface passivation clean

New high-k materials and deposition
- Need: High-K and metal gate tailoring to best performance

New device structure
- e.g. SiGe Nano wire
- Need: Ge/SiGe selective etch

Ultra shallow junction with high surface conformal doping in 3D device structure
- Need: New Doping Scheme

90nm → 45nm → 16nm → 7nm/5nm

Industry Transitioning from 2D to 3D

2D Logic → 3D FinFET
2D NAND → 3D NAND

- Fin and gate size variation can degrade device performance
- 3D NAND reliability depends on device dimension control along deep channels

Source: AMAT
Entegris Uses Electrical Testing To Evaluate Ge Surface Passivation and Queue Time Improvement

Results from Entegris/NCTU Collaboration on Ge Surface Passivation
Stack of Ge Nanowires Formed By Selective SiGe Etching for Ge Mano Wire-Based Gate-All-Around FETs

Before Selective Etch

SiGe/Ge/SiGe/G stack in Fins

Cross-Sectional View of Ge Nano wires

As-received

SG100-X2, 4 minutes 25C

300nm

after Selective Etch

Ge nano wire

source

gate

drain

3D SEM View of Ge Nano wires

After etch removal of SiGe

SiGe: Ge etch > 20:1

Results from Entegris-IMEC JDP on FEOL cleans/etches
As MLD (Monolayer Doping) on Si and Ge Achieved ~Monolayer Coverage Of Doping On Ge Surface

Monolayer Doping Process
- Conformal, damage-free, shallow junction, cost-effective

- Low Temp Silicon-Oxide (SiO$_2$)
- RTA 500°C -1100°C Soak, Spike, Flash Ambient: N$_2$
- Oxide strip (optional)
- DHF (100:1) till Dewet

Figure of Merit for As-MLD in Si and Ge

Ref: Lee et al, SEMATECH Surface Preparation and Cleaning Conference (SPCC), 2015

Results from Entegris-SEMATECH JDA
Device Scaling causing interconnect challenges

- Line resistivity increasing due to Cu electron free mean path and film roughness makes Cu unfavorable as its resistivity will shoot up.
- Reliability issues due to Cu electro-migration below 20 nm
- High aspect ratio features causing yield issues (e.g. voids in plating solution)

Alternative interconnect metals

- Al, Co and W are alternatives
  - display better sheet resistance vs. Cu at <20nm
- Al displays poor EM performance
- Co displays better EM performance
  - can be deposited by ALD, CVD, plating
  - can be integrated into device

Thin film sheet resistance trend W vs. Cu
• WCl₆ purification is critical in achieving good film properties

• Solid delivery vessel enable delivering WCl₆

• Obtained CVD W above 400 °C. Higher temperature required to achieve low resistivity, low impurity level and faster deposition rate.
Selective Co CVD on Cu for Void-Free Via Fill Interconnect

Co Technology In advanced IC: BEOL today and beyond 10nm

Co already being used successfully as barrier and cap. Now we are exploring Co as via contact in 2X/1X high aspect ratio via in BEOL/MOL

CVD Co based Selective Growth for Void Free Via Fill
Ref. Jun-Fei Zheng et al, IITC 21015 (Entegris-Qualcomm-IMEC)

Theoretical simulation shows that Co based via of 3:1 aspect ratio can reduce via resistivity by 30% as compared with Cu filled via with barrier/liner at via size of 10-15nm.
Selective CVD Co Deposition on Cu

Negligible Co on ULK

Confirmed by angle-resolved XPS

Co growth is linear/
no incubation time,
No growth on ULK

Selectivity Co on Cu / Co on ULK >> 300:1
Process Integration

Selective CVD Co Growth on Cu
No Growth of Co on ULK

90nm pitch dual-damascene test structure. Via is 45nm 3:1 aspect ratio

Integration: (a) -> (b) Highly selective via fill by Co selective growth on Cu (c) Big trench structure can be filled by traditional Cu technology

Top View: (a) As-received structure; (b) After Co selective deposition. Process temperature < 300 °C, easily compatible with frontend/M1 process.

Ref. Jun-Fei Zheng et al, IITC 21015 (Entegris-Qualcomm-IMEC)
No Voids/No Seam In Co Filled Via ➔ Fine Grain Suggests Scalability Toward Smaller Bia of 2X/1X nm

(a) High resolution STEM image of the Co filled via. (b) Zoomed image of Co filled via. Note that the grain size is very fine <10nm

Ref. Jun-Fei Zheng et al, IITC 21015 (Entegris-Qualcomm-IMEC)
Wet Removal of TiN Prior To Selective CVD Co Deposition Is Critical

Without TiN wet clean

With TiN wet clean

With TiN wet clean/Top View

Random Defects

No defects

Ref. Jun-Fei Zheng et al, IITC 21015 (Entegris-Qualcomm-IMEC)
Interconnect Metallization Using Electrolytic Cobalt Deposition

enthone® chemistry provides:
- Bottom-Up Fill: 2X/1X nm structures
- Low Resistivity: ≤15 μΩ·cm
- Low Stress
- High Purity: 2-10x VMS purity

- A/R ≥ 8
- Opening ≤ 200 Å
- Co or Cu thin seed layer < 50 Å

Co VMS + ENTHONE chemistry provides:
- Bottom-Up Fill
- Conformal Fill

Co seed
Cu seed

enthone®
Interconnect Metallization Using Electroless Cobalt Deposition

Via pre-fill formulations with pH <9.5 (BEOL) Cu seed

<table>
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<tr>
<th>Parameter</th>
<th>Sample 1</th>
<th>Sample 2</th>
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<td>400°C / 60 min</td>
<td>150 sec / 38.8 nm</td>
<td>150 sec / 41.02 nm</td>
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<tr>
<td>Rs after Anneal</td>
<td>46.6 µΩ-cm</td>
<td>35.55 µΩ-cm</td>
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Optimization ongoing for improved resistivity

Non-selective & fill formulations with pH > 11.5 (MEOL) W seed

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<th>Parameter</th>
<th>Sample 1</th>
<th>Sample 2</th>
<th>Sample 3</th>
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<tr>
<td>Time / thickness</td>
<td>140 sec / 46 nm</td>
<td>120 sec / 37 nm</td>
<td>130 sec / 48 nm</td>
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<tr>
<td>Rs as Plated</td>
<td>22.4 µΩ-cm</td>
<td>18.9 µΩ-cm</td>
<td>22.4 µΩ-cm</td>
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<tr>
<td>450°C / 15 min</td>
<td>15.9 µΩ-cm</td>
<td>13.6 µΩ-cm</td>
<td>17.0 µΩ-cm</td>
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SIMS under ambient conditions

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<tr>
<th>Element</th>
<th>C</th>
<th>O</th>
<th>S</th>
<th>Cl</th>
<th>N</th>
<th>Other</th>
<th>Total impurity</th>
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<td>279.69</td>
<td>2595.28</td>
<td>8.52</td>
<td>0.93</td>
<td>71.87</td>
<td>0.13</td>
<td>2956.42</td>
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Excellent Resistivity

XRD

Using beaker level scale we were able to demonstrate bottom-up via filling capability with candidate formulations mentioned above.
Entegris TiN Clean Solution Has Minimum Co Removal Rate In the BEOL Integration Process

Post final etch

Co capping layer intact after cleaning and exposure to the TiN removal chemical

TK9C showing lowest Co damage of all this customer’s tests

IITC 2015, “Cobalt compatible cleaning solutions for 14nm and beyond”, Courabel et. al.
Advanced materials solutions are critically needed for beyond 10nm technology because of new materials and ever-evolving 3D device architectures.

Device, Equipment, and Material Companies should work together for the very challenge material solutions to reach device performance, yield, and cost targets.

As material solution provider, Entegris is working with device and equipment partners directly or via consortium in the frontier areas with the following examples for beyond 10nm solutions:

- Ge surface passivation by wet chemicals, using electrical MOSCAP as an effective and efficient evaluation vehicle
- Selective wet etch removal of GeSi in GeSi:Ge stack for the formation of Ge nanowires for gate-all-around FinFET at 5nm
- As Conformal monolayer doping on Si and Ge surface achieve doping level that is meeting ITRS targets at 7/10nm
- CVD Fluorine free W deposition for 3D NAND and future logic application
- CVD Co selective growth on Cu for void free Via fill with expectation to work beyond 10nm technology
- Advanced Electrolytic Co plating for replacing Cu in Cu dual-damasence interconnect
- Electroless Co plating as an alternative approach for filling 2X/1X Via on Cu and W bottoms
- Excellent TiN removal without impact to Co in the interconnect integration