Optimizing Equipment Selection for Diverse Fan-Out Process Flows

Tom Strothmann
Director Advanced Packaging Product Development, Kulicke & Soffa Inc.
Scope of the Presentation

• What Defines a Fan-out Package
  – A Wafer Level Package with redistribution layers, mold compound and bumps that extend beyond original silicon die size
  – Packages without a laminate substrate, reducing size and cost
  – Devices predominantly used in mobile products for form factor advantage

• Die Placement in this presentation will be for die placed onto temporary carriers prior to reconstitution
  – Similar processes using laminate will not be covered

• This presentation focuses on one common segment of all fan-out process flows – die placement prior to reconstitution
  – Good example of the dilemma faced by companies making equipment decisions to support a FOWLP manufacturing process
Segments of the Fan-Out Market

• Current or “Core” FOWLP (*typically* eWLB)
  – eWLB (highest volume) / RCP / Deca
  – Lower I/O count devices
  – Mostly single die, some multi-die and a few die with passives
  – Baseband, Power Management, RF, Analog, Bluetooth

• High Density FOWLP
  – *Competing technologies in an unsettled market space*
  – High density I/O capable
  – Application Processors, Memory, Multi-die Si Partitioning, Heterogeneous Integration

• Wafer vs Panel formats and the market drivers for panel realization

• Diverse requirements of the FOWLP market impose significant challenges for equipment manufacturers
  – Particularly true for Die Placement in FOWLP process flows but the diversity extends to other manufacturing segments as well
Diverse FOWLP Market Requirements

• Fan-out Wafer Level Packaging (FOWLP) continues to have the highest growth rate of all Advanced Packaging technologies
• Growth for FOWLP is driven by mobile applications
  – Potential for growth in SiP and IoT packaging is significant
• Process options from low cost single die packages to complex multi-die 3D packages recently driven by Apple and TSMC

*Die placement prior to reconstitution is a key enabling technology*

• Requirements change based on the process flow selected
  – Face up / Face down
  – Die first / Die last
  – Local alignment / Global alignment
  – Low Density I/O / High Density I/O
  – Accuracy 10μm / Accuracy 3μm
  – High force / Low force
  – Heat / No heat
  – Wafer format / Panel format
Multiple FOWLP Die Placement Requirements

Equipment selection is a difficult choice

Panel Face Up
Panel Face Down
Multi-Die
Wafer Face Up
Wafer Face Down
Wafer RDL First
Heat & Force Face Up
Multi-Die & Passives

Accuracy 3μm to 10μm
4000 to 27000 UPH
Tape & Reel Feed
Wafer Film Frame Feed
How to Proceed with Equipment Choice

- Selection of die placement equipment has to balance the specific process flow requirements with UPH and COO considerations.
- Assembly needs can be addressed with specialized equipment architectures optimized for each market segment.

Very High Speed - Combining Active Die and Passive Placement

Select Process Based on Product Requirements

1) FOWLP Product Requirements

2) FOWLP Process Requirements

3) FOWLP Optimized Equipment Requirements

Very High Accuracy and Flexibility

Select Equipment Based on Process Requirements
Available FOWLP Process Flows in HVM Today

- **Face Down, Die First**: Typical Infineon licensed eWLB process, Highest Volume
- **Face Up, Die First**: Similar to flow used by TSMC and others, HVM potential
- **Face Down, Die Last**: Similar to Amkor’s SWIFT or SLIM process
- **Accuracy and UPH are Key Metrics for equipment selection in all flows**
Accuracy Process Tradeoffs

• There is always a trade off for choosing accuracy schemes
• High accuracy vs high throughput
• Thermal process considerations
• Face down typically has the highest position shift but also has the highest UPH (lowest cost)
• Face up die placement accuracy can be improved with application of heat and force to lock die position
• RDL first allows for high accuracy due to metallurgy and die position being locked prior to reconstitution
Accuracy Challenges by Process

• A significant challenge with the FOWLP process is die shift
• Accurately placed die shift position during the reconstitution process due to competing factors
  – Thermal expansion of the carrier material during molding
  – Shrinkage of mold compound during cure
• Placement error is low at center and greater at edge
• Thermal expansion of carrier during placement

Source: Comprehensive Investigation of Die Shift in Compression Molding Process for 12 Inch Fan-Out Wafer Level Packaging Yong Han et. al. IME
Achieving Post Mold Accuracy

- Die drift is not completely modeled. Process tests show that the carrier material, die adhesion to the tape, the mold compound and temperature cycles that occur during bonding and molding all play a role.
- One method that is being employed is to measure the die drift post bond and program the FOWLP bonder to intentionally offset the die.
- Another method is to measure the placed die and adjust the RDL to accommodate the error.
- Pick and place bonding with a heated tool rather than a heated chuck can eliminate one source of error.
- Thermal management measures are critical for High Accuracy die placement.
- Tape and mold compound manufacturers along with bonding companies are working together in collaboration to develop high accuracy post mold placement processes.
Cost Driver Example by Body Size

- Optimized process flow is determined by the needs of the final product.
- Size of the die or size of the final package drives the cost of the process:
  - Optimal process flow is determined by the needs of the final product.
  - Size of the die or size of the final package drives the cost of the process.
  - Wafer dicing and die placement costs are sensitive to die size:
    - Small body or die size adds process time on key equipment.
    - Capacity constraints and added cost.
  - Reconstitution and RDL processing are not die or body size dependent:
    - Fixed price for these processes.
    - Larger body size drives higher fixed cost.
    - Fewer units per wafer or panel.
  - Large body drives panel over wafer.
  - Small die/body drives high UPH for cost:
    - Lower accuracy is acceptable.
    - Fastest die placement is Face Down.

**Bathtub Curve for Process Cost**

- Small Die
- Small Body
- Body Size Sweet Spot
- Large Die
- Large Body
Wafer or Panel Format for Reconstitution?

- The FOWLP manufacturing today is primarily driven by a round 300mm format (or slightly larger)
- Processes and equipment optimized for Wafer Level Packaging can be applied directly to fan-out processes
- Panel format requires new processes and equipment to be developed
  - Panel size has not been set as an industry standard
  - Maximum panel size appears to be 650x650mm but many potential smaller sizes
  - Difficult for equipment suppliers to prepare
  - Immediate TAM is quite low due to die volume per panel
- Panel lines require significant loading for full utilization
- Larger package size is required to drive panel volume (SiP, IoT?)
- Adoption of mainstream panel processing is a few years out

<table>
<thead>
<tr>
<th>Package Size (mm)</th>
<th>Panel Size (mm)</th>
<th>Capacity (panels/wk)</th>
<th>Die/panel</th>
<th>Die/week</th>
<th>Die/year</th>
</tr>
</thead>
<tbody>
<tr>
<td>5x5</td>
<td>300 (round)</td>
<td>1,500</td>
<td>2,490</td>
<td>3.7M</td>
<td>194M</td>
</tr>
<tr>
<td>5x5</td>
<td>550x650</td>
<td>1,500</td>
<td>13,250</td>
<td>19.9M</td>
<td>1,034M</td>
</tr>
<tr>
<td>10x10</td>
<td>300 (round)</td>
<td>1,500</td>
<td>605</td>
<td>0.9M</td>
<td>47M</td>
</tr>
<tr>
<td>10x10</td>
<td>550x650</td>
<td>1,500</td>
<td>3,339</td>
<td>5.0M</td>
<td>260M</td>
</tr>
</tbody>
</table>
Define the Product Requirements

- Passivation opening size (*small passivation opening size drives high accuracy*)
- Number of components (*multi die drives higher accuracy*)
- Value of components (*high value drives die last*)
- Intended package size
  - <5x5mm drives highest speed placement
  - >10x10mm potentially drives panel adoption
- 3D package design (*higher accuracy*)
- RDL L/S ≥ 10μm (*lower accuracy, higher UPH*)
- RDL L/S ≤ 5μm (*higher accuracy*)
- Single or multilevel RDL (*accuracy decision*)
- Single die (*typical high UPH*)
- Multi die (*higher accuracy*)
- Future requirements
## Product Mapping to a Process

<table>
<thead>
<tr>
<th>Product Description</th>
<th>Critical Requirement</th>
<th>Key Attribute</th>
<th>Process</th>
<th>Required Accuracy (3σ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Die Core</td>
<td>Lowest Cost</td>
<td>Highest UPH</td>
<td>Face Down, Die First</td>
<td>7-10μm</td>
</tr>
<tr>
<td>Single Die Core with Passives</td>
<td>Lowest Cost</td>
<td>Highest UPH</td>
<td>Face Down, Die First</td>
<td>7-10μm</td>
</tr>
<tr>
<td>Single Die High Density Hi I/O or Fine Pitch</td>
<td>High Accuracy Lower Cost</td>
<td>Post Place Accuracy</td>
<td>Face Down, Die First</td>
<td>3-5μm</td>
</tr>
<tr>
<td>Multi-Die High Density</td>
<td>High Accuracy Lower Cost</td>
<td>Post Place Accuracy</td>
<td>Face Down, Die First</td>
<td>3-5μm</td>
</tr>
<tr>
<td>Low Value Source Die</td>
<td>Lowest Cost</td>
<td>Highest UPH</td>
<td>Face Down, Die First</td>
<td>7-10μm</td>
</tr>
<tr>
<td>Single Die High Density or High Value Die</td>
<td>High I/O or Fine pitch</td>
<td>Post Place Accuracy</td>
<td>Face Up, Die First</td>
<td>3μm</td>
</tr>
<tr>
<td>Multi-Die High Density or 3D Package Structure</td>
<td>High Yield</td>
<td>Post Place Accuracy</td>
<td>Face Up, Die Last</td>
<td>3μm</td>
</tr>
<tr>
<td>High Value Source Die or 3D Package Structure</td>
<td>High yield</td>
<td>Die Last</td>
<td>Face Up, Die Last</td>
<td>3μm</td>
</tr>
<tr>
<td>High Density Single or Multi Die, High Value</td>
<td>Fine pitch RDL for High I/O</td>
<td>Die Last</td>
<td>Face Down, RDL First</td>
<td>3μm</td>
</tr>
</tbody>
</table>

- Core FOWLP typically lower I/O and smaller die; Baseband, RF, Audio, PMIC, BT
- High Density FOWLP with higher I/O and Larger Die; Processors, Memory, Multi Die SOC
Process Options for the FOWLP Market

- Die Face up or Face Down
- Die First or Die Last
- Single Layer or Multi-Layer RDL
- RDL L/S 10/10 or 2/2
- Single Die or Multi-Die
- 2.5D or 3D
- Passives placed in package

FOWLP Process Options

- Core Face Down Single die
- Core Face Down Multi-die
- Core Face Down with Passives
- High Density Face Down Die First
- High Density Face Up Die First
- High Density Face Up Die Last
- High Density Face Down Die Last

Sources: TechSearch, Yole, TSMC, Freescale, IME
Equipment Selection Guidelines

• R&D operations should select a tool with the most flexibility
  – Trajectory still developing and new options may need investigation
  – Development work is best done in wafer format
• In production processes Accuracy and Productivity are key tradeoffs
• Select the highest speed process available for the planned application
  – High UPH drives lowest cost per unit
• Process with the lowest cost and *adequate* technology wins
• Select Source die input
  – Wafer film frame, Tape & Reel, Waffle Pack, JEDEC Tray
• Single die or multi-die requirements in the planned products
• Future product requirements
Equipment Continuum

<table>
<thead>
<tr>
<th>Accuracy &lt; 5μm</th>
<th>5 μm to 10 μm</th>
<th>Accuracy &gt; 10 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>APAMA – FOWLP, TCB, Flip Chip</td>
<td>Hybrid – FOWLP, Flip Chip, SiP</td>
<td></td>
</tr>
</tbody>
</table>

Advantage of Accuracy
FOWLP Flow Flexibility

Clear Advantage for UPH
Passives and Active Die Placement

4,000 UPH @ 3 μm
FC or FOWLP
Face Up / Face Down
Wafer Recon Format

12,000 UPH @ 7 μm
FC or FOWLP
Active and Passives
Wafer or Panel Recon Format
K&S Hybrid Attributes

- HVM system with very high speed
- Actives and Passives in one system
- Active Accuracy +/- 7μm, 12K UPH
- Passive Accuracy +/- 25μm, 100K UPH
- Face Down or Face Up die placement
- Global or Local Alignment
- Die Input: Tape & Reel, Cassette Wafer Feeder, JEDEC Tray
- Flux Dip Capability
- Die placement on wafer
- Die placement on panel
  - Max 450mm panel width
- Low Force Capability
- Optimized for Core FOWLP
**K&S APAMA Attributes**

- Die Placement for all FOWLP Flows
- Highly Accurate die placement
  - ± 3μm for FOWLP or FC
  - ± 2μm for TCB capability
- UPH 4K at 3μm, 5K at 5μm
- Die placement on round format
- Face Up or Face Down
- Global or Local Alignment
- Heated die placement
- Heated chuck option
- Flux dip capability
- Thin die handling
- Optimized for HD FOWLP
- Future protection
Conclusions

• FOWLP technology has numerous competing process options

• Equipment selection has to be analyzed by process segment
  – Driven by required capability and FOWLP unit cost

• The selection process is logically sequential
  1. Define the current and future Product Requirements
  2. Select the Process Flow best suited to the intended product
  3. Select the Equipment best optimized for the Process Flow
  4. Evaluate vendors based on Technology, Cost of Ownership and Support capability (technology requirements will change)

• HVM will be dominated by round wafer format for the next few years

• Panel processing will ultimately be driven by package size and required process capability
Thank You!