Embedded Packaging Technology – The Opportunities and Challenges

Huili FU
Chief IC Packaging Expert, Hisilicon
The Driving Force for Embedded Pkg Technologies
Driving Force

- Embedded packaging?
  - From system point of view, all (almost) packages are embedded packages

- Why we need to re-address the embedded packaging technologies?
Driving Force

- The scale gap

With the wafer process progress, the gap between the nano-world and reality increasing.
Driving Force

- The space budget (Margin)
  - Space margin needed separately for front-end and back-end for traditional business model
  - No more DOUBLE space margins for due to system integration density demand

- Embedded packaging technologies is to solve the space margin problem

- System integration density demand / space margin drives embedded technologies

Space budget is the key driver. Embedded technologies is the one but not the only one to solve the problem.
Driving Force

- **Low power**
  - Shorter interconnections leads to low power
  - Power supply efficiency improves

- **EMI noise reduction**
  - Conformal shielding with zero footprint increase
  - Highly integrated compartment shielding for mixed digital and RF applications

Performance improvement is the demand for the adoption of the embedded technologies.
Embedded Opportunities and Challenges
Fan-out

- Opportunities
  - Inherently embedded solution – bridge the scale gap
  - Multi-die integration
  - Heterogeneous integration
  - Time to market
  - Yield improvement (by die partition)
Fan-out

- **Challenges**
  - Mid-end manufacturing capability
  - Warpage control
  - Fine/line space (for die to die interconnection)
  - Cost and Yield
  - Accurate patterning (for fine pitch layout in wafer/panel level operation)
  - Reliability (board level)

Fine line interconnection (L/S 2/2um)

Fine line strength

Wafer level warpage control
Fan-out

Application considerations

- **Mobile/IoT**
  - Multi-function integration: PMIC/RF/BB/AP/Connectivity (Single die or SIP)
  - Small form factor (Thinner and smaller)
  - Engineering issues: package strength, board level reliability
  - Cost competitiveness

- **Networking/CPU**
  - Heterogeneous dies integration: server + memory: die partition
  - Large package size
  - Fine line space
  - Thermal and reliability issue
  - Cost benefit
Substrate Embedded Pkg

- Opportunities
  - Small form factor
  - Low profile (Si thickness down to 50um)
  - Sub-system / small system integration (including discrete components)
  - Better performance

Embedding IC saves PCB area up to 38% compare to High-density PCBA

Ultra thin IC (Die grinding down to 50um)

Multi-Die embedded technology combine with conventional DB process lead to various sub-system in SIP format
Substrate Embedded Pkg

- **Challenges**
  - High-density substrate implementation
  - Process & material
  - Reliability (Moisture, Delam)
  - Yield / cost

All the defect in the substrate process will introduce yield loss.

<table>
<thead>
<tr>
<th>Failer Mode</th>
<th>Defect 1</th>
<th>Defect 2</th>
<th>Defect 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Abnormal circuit pattern</td>
<td>Foreign material</td>
<td>Short</td>
</tr>
</tbody>
</table>

Resin Film Void between Die and polymer layer

Die chipping by X-section

High-density substrate can not be used here

L/S: 50um/50um
Substrate Embedded Pkg

- Application considerations
  - Mobile/IoT
    - PMIC/RF/BB/Connectivity (Single die or SIP)
    - Small form factor (Thinner and smaller)
    - Engineering issues: substrate process and chip compatibility
    - Cost competitiveness
High-density substrate technology

Opportunities
- Existing assembly process
- Panel/strip level technology for low cost
- Known-good-substrate assembly for better yield
- Better reliability

Panel level vs. wafer level for low cost

High-density substrate development

AOI & ICT test for KGS assembly
High-density substrate technology

- **Challenges**
  - Thickness—difficult to implement very thin sub.
  - Fine line assembly
  - Large panel & fine pitch manufacturing
  - Fine pitch manufacturing environment control
  - ELK stress issue

Structure and Material combination used for fine pitch substrate prone to larger stress problem

<table>
<thead>
<tr>
<th>DoE for different combination</th>
<th>DoE1</th>
<th>DoE2</th>
<th>DoE3</th>
<th>DoE4</th>
</tr>
</thead>
<tbody>
<tr>
<td>ELK stress on bump top ratio @DB</td>
<td>1X</td>
<td>1.03X</td>
<td>1.06X</td>
<td>1.2X</td>
</tr>
<tr>
<td>Bump stress ratio @ DB</td>
<td>1X</td>
<td>1.06X</td>
<td>1.08X</td>
<td>1.24X</td>
</tr>
<tr>
<td>Die corner stress ratio @ TCT</td>
<td>1X</td>
<td>1.02X</td>
<td>1.04X</td>
<td>1.18X</td>
</tr>
<tr>
<td>Bump stress ratio @ TCT</td>
<td>1X</td>
<td>1.01X</td>
<td>1.05X</td>
<td>1.19X</td>
</tr>
</tbody>
</table>

DOE1: Structure and Material combination for L/S 15/15
DOE2: Structure and Material combination for L/S 7/7
DOE3: Structure and Material combination for L/S 5/5
DOE4: Structure and Material combination for L/S 2/2
High-density substrate technology

Application considerations

- **Mobile/IoT**
  - Multi-function integration: PMIC/RF/BB/AP/Connectivity (Single die or SIP)
  - Small form factor (smaller and relatively thin)
  - Engineering issue: ELK stress
  - Cost competitiveness

- **Networking/CPU**
  - Heterogeneous dies integration: server + memory; die partition
  - Large package size and warpage control
  - Cost benefit
Concluding Remarks
Concluding Remarks

- From system point of view, (almost) all packages are embedded packages.

- With the evolution of wafer process, the gap between wafer nano-scale and reality increases, bringing huge challenges to IC packaging technology.

- Space budget is key demand. Embedded is one but not the only one to solve the space budget problem.

- In the era beyond Moore's law, embedded package technologies will be an important way to extend the Moore's law in the package level.
Thank You

---

QUESTIONS?