Markets

- Mega trend – exploding data and interconnectivity
  - More end users
  - IOT – more end devices
  - 5G – more data per user
- Data center – Cloud Service Providers (CSP)
  - Consolidation and virtualization
  - Networking
    - Switches and routers
  - Servers (CPUs)
  - Photonics
- Telephony (5G)
- High performance computing

50 Billion Devices by 2020

25 Million Cloud-based Servers
IC Packaging Evolution – System Considerations

**Performance**
- Higher memory bandwidth
- Lower power

**Cost Reduction**
- Advanced silicon node cost avoidance
- Integrate heterogeneous die

**Board Space**
- Single package platform
- Reduce floor space
Amkor’s Multi-die TSV Packages

2.5D FCBGA
- 2.5D TSV Flip Chip BGA
  - Homogenous & heterogeneous die integration
  - Multi-die, side by side
  - < 2 µm L/S D2D
  - Bare die, overmold, lidded

3D-TSV
- 3D TSV Flip Chip BGA
  - Logic/Logic and Logic/Memory configurations
  - High performance
  - No mold

3D-TSV DRAM
- DRAM stacking
- Molded
- Bare die & exposed die
Assembly Process Flexibility

- **Multi-die construction versatility**
  - 2.5D TSV (Logic + Logic, Logic + Memory, Logic + Memory + discrete IO die)
  - 3D TSV Logic + Memory
  - 3D TSV Logic + Logic
  - DRAM stacking
  - Other component types: Analog, MEMs, Sensors

- **Key factors**
  - System size (interposer and die sizes) – trend is larger
  - Electrical signaling and Power-Deliver-Network (PDN)
  - Device power
  - Electrical test and test points – interim test or not
  - Cost optimization
Multi-Die Platform and Process Intersections

**COS (Chip-on-Subst.)**
- Lowest cost
- Strong leverage of FPGA assembly

**COW – No Mold**
- Large die sizes
- Thin core substrates
- Enables interim electrical test

**COW – Molded**
- Large die sizes
- Thinner core substrates

**Typical 2.5D TSV Product**
- Surface mount on board
CoS Process Flow

• No molding
  – Interim test available
  – Mold sensitive components OK
• Shared infrastructure with FCBGA
CoS Warpage Mitigation

- Initial interposer warpage affects the PCB + interposer warpage
- For the successful top die attach warpage minimization of interpose is important
- Inorganic C4-side passivation layer can reduce interposer warpage.
- Warpage control requires tuning the C4-side passivation (see MEOL process 1, 2, 3 below)

![Graph showing warpage control and tuning range](image)

**Good tuning range**
MEOL Process

1. Wafer Thinning

2. Si recess (Dry etch)

3. Passivation (PECVD)

4. TSV Reveal (CMP)

5. UBM/C4 Bump

0. Carrier Bonding (WSS)

Device Wafer

- carrier
- Release layer

6. Carrier De-Bonding

Finished TSV Wafer

C4 Bumped Wafer
Proven 2.5D CoS (Chip-on-Substrate) Process

COS Process Flow (Chip-on-Subst.)

- COW – No Mold
- COW – Molded

Proven 2.5D POR Process

2.5D TSV - COS

- Logic
- HBM

Graph:
- Y-axis: Logic (large die) area (mm²)
- X-axis: Si interposer area (mm²)
- Points:
  - L: Logic die size
  - I: Si interposer size
  - CoS
  - Reticle size
  - L: 26 x 22 mm
  - L: 26 x 20 mm
  - L: 22 x 18 mm
  - I: 36 x 28 mm
  - I: 33 x 27 mm
  - I: 32 x 26 mm

Standard Substrate
# 2.5D Product Experience/TV Floor Plan

<table>
<thead>
<tr>
<th>Applications</th>
<th>Platform</th>
<th>Graphics/HPC/Network</th>
<th>Network/Server</th>
<th>FPGA</th>
<th>Network/Server</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interposer</td>
<td>Si</td>
<td>Si</td>
<td>Si</td>
<td>Si</td>
<td>Organic</td>
</tr>
<tr>
<td>Logic</td>
<td>40/28 nm</td>
<td>28 nm</td>
<td>28 nm</td>
<td>28 nm</td>
<td>40/45 nm</td>
</tr>
<tr>
<td>Memory/ small logic</td>
<td>DRAM</td>
<td>HBM (x2/x4)</td>
<td>RLDRA (x1/x4)</td>
<td>SerDes</td>
<td>HBM / TV</td>
</tr>
<tr>
<td>Status</td>
<td>Qualified</td>
<td>Qualified</td>
<td>Completed Reliability/ Functional Demonstration</td>
<td>Demonstrated/ LVM 2013</td>
<td>Under Development</td>
</tr>
</tbody>
</table>

**Floor plan**

- **Substrate**
- **Si interposer**
- **Organic Interp.**
- **Logic**
- **Memory/ Small logic**

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[Image of floor plan]
# 2.5D MCM TSV Using CoS Options

<table>
<thead>
<tr>
<th></th>
<th>Product 1</th>
<th>Product 2</th>
<th>Product 3</th>
<th>Product 4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Package type</strong></td>
<td>2.5D TSV FCBGA</td>
<td>2.5D TSV FCBGA</td>
<td>2.5D TSV FCBGA</td>
<td>2.5D TSV FCBGA</td>
</tr>
<tr>
<td><strong>Package dimensions</strong></td>
<td>45 x 45 mm</td>
<td>55 x 55 mm</td>
<td>50 x 50 mm</td>
<td>25 x 25 mm</td>
</tr>
<tr>
<td><strong>Interposer size</strong></td>
<td>26 x 32 mm</td>
<td>28 x 36 mm</td>
<td>26 x 32 mm</td>
<td>21.5 x 22.0 mm</td>
</tr>
<tr>
<td><strong>Logic die size</strong></td>
<td>19.5 x 26.0 mm</td>
<td>22 x 26 mm</td>
<td>18 x 18 mm</td>
<td>5.0 x 12.7 mm</td>
</tr>
<tr>
<td><strong>Memory size</strong></td>
<td>5.48 x 7.29 mm</td>
<td>5.48 x 7.29 mm</td>
<td>9 x 9 mm</td>
<td>10.9 x 16.0 mm</td>
</tr>
<tr>
<td><strong>Memory type</strong></td>
<td>4 placements</td>
<td>4 placements</td>
<td>2 placements</td>
<td>1 placement</td>
</tr>
<tr>
<td><strong>Moisture sensitivity</strong></td>
<td>MSL4 90/90 90/90 90/90 30/30</td>
<td>MSL4 225/225 MSL4 50/50 50/50</td>
<td>MSL3 20/20 90/90</td>
<td>130°C/85% 96 hrs n/a 45/45</td>
</tr>
<tr>
<td><strong>Highly accelerated</strong></td>
<td>110°C/85% 264 hrs 419/419 130°C/85% 96 hrs 25/25 25/25</td>
<td>130°C/85% 96 hrs n/a 45/45</td>
<td>440/440 T/C-B 1000x 25/25 25/25</td>
<td>46/46 T/C-B 2000x n/a 25/25</td>
</tr>
<tr>
<td><strong>Temperature cycling</strong></td>
<td>T/C-B 1200x 45/45 30/30 T/C-B 1000x 25/25 25/25</td>
<td>T/C-B 1000x 20/20 25/25</td>
<td>T/C-B 2000x n/a 15/15</td>
<td>T/C-B 2000x n/a 15/15</td>
</tr>
<tr>
<td><strong>High temperature</strong></td>
<td>150°C 1000 hrs 45/45 45/45 45/45</td>
<td>150°C 1000 hrs 30/30 150°C 1000 hrs 25/25 25/25</td>
<td>150°C 1000 hrs 25/25 25/25</td>
<td>150°C 1000 hrs n/a 15/15</td>
</tr>
</tbody>
</table>

**Electrical and FA Confirmed**
CoW Process

Top die attaching on interposer wafer!

- Chip on substrate (COS)
  - Die attached to interposer + substrate
  - Better suited for >> reticle sized interposers
  - Mold encapsulation is not possible
  - No need for flip bonding/ de-bonding process

- Chip on wafer (COW)
  - Die stack on flat wafer surface
  - Stable assembly line yield
  - Better UPH in wafer level chip attach & UF processing
  - Encapsulation with EMC is possible (COW molded)

Same target, different method!
Multi-die Platform and Process Intersection

- Larger interposers, larger die, thinner substrates
- Permits Interim test & mold-intolerant parts (no-mold)
- Qualification 2016

COS

COW – No Mold

COW - Molded

2.5D TSV - COW

- Logic (large die) area (mm²)
- Si interposer area (mm²)

Reticle size

L: Logic die size
I: Si interposer size

Both CoS and CoW

L: 26 x 22mm
I: 36 x 28mm

L: 25 x 20mm
I: 35 x 27mm

L: 22 x 18mm
I: 32 x 26mm
CoW Chip Last Process Flow

**CoW Chip Last Process Flow**

- **TSV interposer and front pad**
- **Carrier bond, TSV reveal, BS RDL & C4**
- **Re-bond to back side (=C4 side)**
- **Front side carrier de-bond**
- **CoW top die attach and underfill**

**Non-mold CoW**
- Interim test flow available
- Interposer backside process first then top die attach

**Mold last CoW**
- Thinner interposers
- Interposer backside process first then top die attach

- **Wafer mold and mold side grind**
- **Carrier de-bond and dicing**
- **Sub-assembly to substrate**
Typical Warpage Behavior of CoW Process

- No risks in top die attach on interposer regardless of die size
- Top die + interposer module attach on PCB is the key process
- For the successful module attach, module structure with material is important

![Diagram showing warpage behavior](image-url)
## 2.5D CoW Product Experience/TV Floor Plan

<table>
<thead>
<tr>
<th>Applications</th>
<th>Graphics/HPC/Network, K1</th>
<th>Graphics/HPC/Network, S1</th>
<th>Network/Server, UTV</th>
<th>Network/Server, K1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package type</td>
<td>Non Mold, CoW</td>
<td>non-Mold CoW</td>
<td>Mold, CoW</td>
<td>Mold, CoW SLIM™</td>
</tr>
<tr>
<td>Interposer</td>
<td>Si</td>
<td>Si</td>
<td>Si</td>
<td>Si (No TSV)</td>
</tr>
<tr>
<td>Logic</td>
<td>18 x 18 mm, 28 nm</td>
<td>26 x 20 mm, 28 nm</td>
<td>28 nm (11.2 x 14 mm x 2)</td>
<td>28 nm (18 x 18 mm)</td>
</tr>
<tr>
<td>Memory/ small logic</td>
<td>DRAM (x2)</td>
<td>HBM (x4)</td>
<td>DRAM (x4)</td>
<td>DRAM (x2)</td>
</tr>
<tr>
<td>Status</td>
<td>Reliability validated</td>
<td>Reliability validated</td>
<td>Development</td>
<td>Development</td>
</tr>
<tr>
<td>Floor plan</td>
<td><img src="image" alt="Substrate" /></td>
<td><img src="image" alt="Si interposer" /></td>
<td><img src="image" alt="Organic Interp." /></td>
<td><img src="image" alt="Logic" /></td>
</tr>
</tbody>
</table>

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**Semiconductor Technology**

**Amkor Technology**

**Semi**
SLIM™ with CoW

- Silicon-Less Integrated Module (SLIM™)
  - Foundry BEOL layers retained
  - No TSV – lower cost
  - High interest by high performance & networking customers

- SLIM Value Proposition
  - 20% lower cost than TSV
  - Damascene yields already established and > 99.5%
  - Better electrical performance
    - Lower insertion loss on-package
    - Highest off package signaling
  - Extremely thin
    - Integration into NEW product concepts is possible
MCM Integration Using SLIM™

- FinFET + 28 nm (2 die) w/o substrate + DRAM
- Amkor TV: 15 mm TV, 2 die, 2L Cu BEOL+1L RDL, 0.4 mm pitch I/O, 4800 \( \mu \)-bump/die, 100 \( \mu \)m D2D spacing

Die 1

Fine pitch u-bump joints (30~40 \( \mu \)m) connected via BEOL Cu + RDL Cu for die to die interconnection

BGA for SMT

TMV solder for memory stack

Package level reliability
- Passed preconditioning MSL3/260
- Passed TC ‘B’ 1000x
- Passed uHAST 192 hrs

Board level reliability
- Passed 2000 TC cycles
  - JEDEC condition G in JESD22-A104
- Passed 1000 drops
  - JESD22-B111 compliant board
- In-situ monitored

Amkor TV cross section
Conclusion

• Increased demand for high performance applications has required assembly of multiple large die
• 2.5D TSV has provided this high performance multi-die path
• Large interposer sizes and large functional die sizes demand flexibility from the assembly processes to achieve excellent yield
• Currently two approaches CoS/CoW are mainstream for Amkor
  • CoS process leverages standard FCBGA processes and allows interim test before HBM attach and initial warpage control of interposer is the key concern in CoS success
  • CoW enables larger top die attach joining first, to take advantage of very flat silicon interposer and extend the process envelope beyond that for COS
• Amkor is adopting both technologies to provide high quality high performance packages in 2.5D/3D/Photonic device applications
Thank You