FO-WLP, Embedded Die, and Alternatives: Market Trends and Drivers
Many Package Choices: Which One is the Correct Choice?

- FO-WLP (chip-last, chip-first, face-up, face-down)
- Traditional flip chip on laminate substrate, new versions with coreless substrates or thin core substrates
- Embedded die
Fan-Out WLP and Embedded Die Technologies

Mainstream - black
Exceptions - red
Examples - blue

Embedded Packaging Technologies

Die Embedding in Organic Laminate
"Embedded Die"

- Fan-In Type
  - Chip-First
    - NA
  - Chip-Last
    - ECP (ATS)
    - SESUB (TDK)
    - i²Board (Schweizer)
    - i²Pack, µ²Pack (Schweizer)
    - WFOP (J-Devices)
    - BLADE (Infineon)
    - BossB2it, B2itPWB (Dai Nippon)
    - ChipsetT/ChipletT (FlipChip/TSHT, Fujikura)
    - aEASI (ASE)
    - EOMIN (Taiyo Yuden)
    - Clover embedded device (Unimicron)
    - MCEp (Shinko)
    - EMBI/Si-Bridge (Intel)
    - EWLP (Imbera)

- Fan-Out Type
  - Chip-First
    - EMAP (GTPRC)
  - Chip-Last

Die Embedding in Epoxy Moldcompound
"Fan-Out WLP/PLP"

- Fan-In Type
  - Chip-First
    - eWLB, aWLP, WLFO (Infineon, JCT STATS ChipPAC, ASE, NANIUM)
    - RCP (Freescale/NXP, Napes)
    - M-Series (DECA)
    - InFO (TSMC)
    - WLFO (Amkor)
    - ADL/SinoChip
    - FOWLP (SPIL)
    - NTI (SPIL)
    - WFP (Samsung)

- Fan-Out Type
  - Chip-First
  - Chip-Last

Solutions that can be categorized as Advanced Flip Chip technologies:

- FOCLP (ASE)
- SWIFT (Amkor)
- SLIM (Amkor)
- RDL-First FOWLP (IME)
- HDL (QPL)
- FC-MISBGA (SPIL)
- EMBI/Si-Bridge (Intel)

Source: Steffen Kroehnert, NANIUM
Why FO-WLP?

- Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)
- Thinner than flip chip package (no substrate)
  - Can enable a low-profile PoP solution as large as 15mm x 15mm body or greater
- Support increased I/O density
  - Fine L/S (10/10µm)
  - Roadmaps for <5/5µm L/S, future 2/2µm L/S
- Allows use of WLP with advanced semiconductor technology nodes with die shrinks
  - With increased I/O and smaller die can’t “fan-in” using conventional WLP
  - Smaller diameter balls and ball pitch ≤0.3mm board level reliability issues (Qualcomm studies)
- Split die package or multi-die package/SiP
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- Excellent electrical and thermal performance
Process Flows for the Various FO-WLP Approaches

Traditional WL-FO
- Face Down Die Placement
- Molding and Carrier Removal
- RDL and BGA Attach
- Singulation

Die First HD-FO
- RDL and Cu Pillar on Carrier
- Face Up Die Placement
- Molding, Thinning/Cu Via Exposure
- RDL and BGA Attach
- Carrier Removal

Die Last HD-FO
- RDL on Carrier
- Face Down Die Placement
- Molding
- Carrier Removal, RDL and BGA Attach
- Singulation

Application Processor: A Case Study

- **Thinner package and smaller footprint**
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- **3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out (thermal, cost, business issues)**
- **Silicon interposers too expensive for many mobile products**
- **PoP in high-end smartphones**
  - Option 1: Continue with FC on thin substrate
  - Option 2: Embedded AP in bottom laminate substrate
  - Option 3: Fan-out WLP with application processor as bottom package
  - Option 4: Some new format (RDL first/chip last, SWIFT, etc.)
- **Apple selects InFO for AP in bottom PoP**
  - Low profile
  - High routing density
  - Improved electrical and thermal performance
  - System integration with competitive cost
  - Co-design is key

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**Today’s PoP (1.0mm)**

**FO-WLP as Bottom PoP (<0.8mm)**
RF, PMIC, CODEC and AP, Migrating to FO-WLP

- Modem FCBGA-333
  Qualcomm MDM9625M
- RFIC WLP-164
  Qualcomm WTR1625L
- RFIC WLP-66
  Qualcomm WFR1620
- Audio codec
  WLP-42
  Cirrus 338S1201
- WIFI/BT/FM
  FLGA-58
  Murata 343S0694
- Modem FCBGA-267
  Apple/TSMC APQL-
- M8 Co-pro. WLP-40
  NXP LPC18B1UK
- PMIC WLP-94
  Qualcomm PM8019
- PMIC FCBGA-267
  Dialog 338S1251
- PMIC WLP-28
  Qualcomm QFE1100

Source: TPSS.
Alternatives to Reconstituted Wafer FO-WLP: Select the Right Solution for Your Application

- Amkor’s SWIFT
- ASE’s FOCLP
- Amkor’s LCCSP
- Conventional flip chip
- Molded Interconnect Substrate (MIS)
- Embedded die solutions

Source: Infineon.

Source: Amkor.

Source: ASE.

Source: TDK.

Source: SPIL.
ASE’s FOCLP

- **Uses low-cost coreless substrate**
  - Fine pitch capable (15µm L/S, 12µm L/S in development)
  - Manufactured in double panel format
  - Assembled in strip format
  - Multi-die and passives possible
  - Can be bottom PoP

- **Thin package (<375 µm)**

- **MLS-1**
  - Passed TCT 1,000 cycles, PCT 168 hours, HAST 168 hours, Drop test 150 (still going)

- **High current and thermal handling capabilities**
  - Due to thicker Cu (15-20 µm)

- **Uses existing FC infrastructure**
  - FC with Cu pillar (direct die on pad, no RDL) mounted on coreless substrate
  - Mass reflow and molded underfill

Source: ASE.
Amkor’s LCCSP

LCCSP Building Blocks
- fcCSP w/ Low Cost Sub
- 1.5 and 2 Layer Options
- Coreless Prepreg (ETS)
- Molded Substrate (MSP)

Typical Die Sizes Range From 3-7mm

LCCSP Benefits
- 6 Sided Silicon Protection
- Improved BLR for Low K Si
- Large Installed Capacity Base
- Post Assembly (Final) Test

Source: Amkor.
Molded Interconnect Substrate

- MIS-BGA offered by JCET (owns APS), Carsem, SPIL and others
- Versions offered by other OSATs such as Amkor and UTAC with routable QFNs

Source: JCET.
- Leadframe supplied by leadframe maker using special process
- Limited number of leadframe suppliers capable of supplying
SPIL’s FC-MISBGA Package  
(Flip Chip – Molded Interconnect System BGA)

- Coreless substrate (no copper clad laminate core)
- Embedded trace technology: better trace adhesion to substrate dielectric layer
- Fine trace: \( L/S=20/20\mu \text{m}, 15/15\mu \text{m} \) trace formed by embedded trace technology, not SAP
- Molding compound replaces prepreg
- Trace routability
- Little warpage
- Excellent electrical performance
- Good thermal and reliability performance
MIS-BGA in Production

- **MediaTek uses for**
  - RF transceiver
  - Power management IC (PMIC)
- **China mobile phones such as OPPO Joy**
- **MediaTek RF transceiver**
  - Wire bonded die
  - Body size 4.6 mm x 4.6 mm x 0.8 mm
  - 104 solder balls
  - Ball pitch 0.4 mm
- **MediaTek PMIC**
  - Wire bonded die
  - Body size 6 mm x 6 mm x 1.0 mm
  - 145 solder balls
  - Ball pitch 0.4 mm
- **Considered low-cost package**

Source: TPSS and TechSearch International, Inc.
Embedded Active Package Solutions

- ASE Embedded Electronics (including new JV company with TDK)
- AT&S
- DNP
- General Electric
- Infineon
- Microsemi
- Schweizer
- Shinko Electric
- Taiyo Yuden
- TDK
- Texas Instruments
- Unimicron

Source: TI.

Source: Chipworks

Source: TDK.

Source: TI.
Qualcomm Snapdragon with Embedded Die

- Snapdragon series
- Many smartphones
AT&S Embedded Component (ECP®)

Current High Volume Production

Power Management

Embedding passives and ICs
- Advantages
  - Reduced form factor X, Y & Z
  - Lower Loop Inductance
  - Improved thermal
  - Improved reliability
- Experience - 5 years volume production in a laminate panel process

Near Future High Volume Production

3D SiP and Modules

Higher Power >500W

In Development

Increased 3D Complexity
All in One Package
TDK’s SESUB Technology for SiP

SESUB = Semiconductor Embedded in SUBstrate

- IC wafer is thinned to 50µm and IC is embedded in resin substrate
- Total substrate thickness is 300µm

Source: ASE, TDK.
TDK Embedded Die Applications

- Apple TV uses μDCDC modules in the remote controller (two per board)
- Low-energy Bluetooth module
  - Ultra small package 4.6 x 5.6 x 1.0mm
  - TI’s CC2541 IC inside substrate
- Bluetooth module
  - Dialog’s DA 14580 embedded in substrate
  - TI’s CC2541 IC inside substrate
- Typical uses and applications
  - Healthcare/Sports & fitness equipment
  - Wearables such as wristband, watch, ring glasses, shoes, hat, shirt
  - Home entertainment equipment (remote control, sensor tag, toys, lighting)
  - PC peripherals (mouse, keyboard, stylus, presentation pointer)

Source: iFixit
TDK’s Tiny Bluetooth Low Energy Module for Smart Watches and Other Wearables

- Bluetooth low-energy module with IC embedded into thin substrate, peripheral circuitry includes quartz resonator, bandpass filter, and capacitors on the top
- Package size of 4.6 mm x 5.6 mm x 1.0 mm
- 65% smaller than individual discrete components

Source: TDK.
Microsemi Embedded Die Module for ICD

• Qualified to MIL standard for implantable devices
• Applicable in other high-rel spaces such as wearables, security, military, and industrial sensing
• Evolution toward ultra-thin embedded die, enabling lamination thickness of 0.5 mm; overall module height typically 1.0 mm (discrete component limit)
• Integrated passives on the horizon

New embedded die design reduces area 400%

Die embedded in the PCB

12.7 mm x 8.1 mm x 1.5 mm

Source: Microsemi.
Conclusions

• Mobile devices drive thinner packages
• No single package meets all needs, multiple choices for same application
  – FO-WLP
  – Flip chip on thin core or coreless
  – Embedded die
• Companies want to use the lowest cost package
• Must calculation trade-off in performance vs. cost
• Companies want to avoid confusion about package choices......
Thank you!

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