Interposer Technology: Past, Now, and Future

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3D TSV: Have We Waited Long Enough?

• Garrou (2014): “A Little More Patience Required for 2.5/3D”
  – All things come to those who wait

• In 2016, interposer-TSV has grown into a steady 3DIC business
  – 4 years after the 1st CoWoS product
  – Huge efforts spent in perfecting the technology, plus HBM as a key add-on
Why Interposer But Not Yet 3D IC?

• Interposer SIP:
  – Node independent: TSV in a mature, interconnect-only chip
  – High yield: Enjoy fab-class, low $D_0$ wafer process
  – Thermal friendly: Directly leverage existing thermal solutions

• Logic-based 3DIC:
  – Node dependent: TSV insertion in advanced Si node
  – Yield concern: Ability for KGD before stacking
  – Thermal: High power density requires innovative thermal solutions
Homogeneous CoWoS® SIP

- **Chip Partition**
  - Break one large die into smaller dies of the same functions
  - Significant yield benefit to justify the integration cost

\[
\text{Yield} = \exp(-D_0 \times A)
\]

- \( D_0 = D/2 \text{ in}^{-2} \)
- \( D_0 = D \text{ in}^{-2} \)

![Diagram showing chip partition and yield relationship](image-url)
Heterogeneous CoWoS® SIP

• Logic chips of different functions and nodes
  – Cost saving from core chip partition and lower cost IO chip
• Logic-memory integration
  – A long missed goal in both SoC and SIP
  – Performance, power, and form factor
Interposer CoWoS® Application Space

- **CoWoS®**
  - High performance SoC partition
  - Stacked memory (HBM) compatible
  - Very high pin count (>3000)
  - Extremely high performance
  - Cloud servers, super computers

- **InFO**
  - Multi-chip integration
  - Small form-factor
  - Cost competitive
  - End-user devices

- **Package Size, mm²**

- **IO Ball Count**

- **Clear differentiation between interposer-TSV and fan-out technologies**
1\textsuperscript{st} Generation CoWoS®

- Production starts with 28nm logic chips (2012)
- Homogeneous and heterogeneous interposer up to 800 mm\(^2\) (Full reticle size)

Courtesy of Xilinx
Fast Time-to-Market for New Si Nodes

- Demonstrated industry’s first 16nm network processor on CoWoS® module (2014)
- **Fast time-to-market** is achieved by interposer SIP, which eliminates node-dependent CPI seen in conventional packages
2nd Generation CoWoS® Development

Interposer 1200 mm²
(~1.5x reticle size)

3D memory integration

Better scalability
Reduced mismatch

Enhanced power integrity

CoWoS XL
HBM Integration
Cu C4 bumps
HD MiM Caps

2nd - Gen. CoWoS
2nd Generation CoWoS®: CoWoS-XL1

- Extra large interposer ~1200 mm²
- Composed by two-masks stitching of sub-micron RDL
- Package with record-large chip size
- Passed stringent component reliability tests

XCVU440
20B X'stores

Courtesy of Xilinx
HBM1 Gen1 vs. Gen2

<table>
<thead>
<tr>
<th></th>
<th>HBM1</th>
<th>HBM2</th>
</tr>
</thead>
<tbody>
<tr>
<td>JEDEC standard</td>
<td>JESD235</td>
<td>JESD235A</td>
</tr>
<tr>
<td>Stack size (mm x mm)</td>
<td>~5.5 x 7.3</td>
<td>~8.0 x 12</td>
</tr>
<tr>
<td>Total z height (um)</td>
<td>480</td>
<td>720</td>
</tr>
<tr>
<td>Number of uBump</td>
<td>4942</td>
<td>4942</td>
</tr>
<tr>
<td>Bandwidth per stack</td>
<td>128 GB/s</td>
<td>200 - 256 GB/s</td>
</tr>
<tr>
<td>4-Hi Capacity</td>
<td>1 GB</td>
<td>4 GB</td>
</tr>
<tr>
<td>8-Hi Capacity</td>
<td>N/A</td>
<td>8 GB</td>
</tr>
<tr>
<td>Availability</td>
<td>2015</td>
<td>2016</td>
</tr>
</tbody>
</table>

- HBM2 has far better density and bandwidth than HBM2

Sources: SK hynix & Samsung
2nd Generation CoWoS®: CoWoS-XL2

- 1st interposer-HBM2 product (2016)
  - 16nm SoC chip + 4 HBM2 (16 GB)
  - 1200 mm² interposer size
  - 300 W power consumption
  - 150B transistors total, 15.3B on SoC
  - Core of deep learning supercomputer

Higher Memory Bandwidth

<table>
<thead>
<tr>
<th>GDDR5</th>
<th>HBM2</th>
</tr>
</thead>
<tbody>
<tr>
<td>288 GB/s</td>
<td>720 GB/s</td>
</tr>
<tr>
<td>12GB GDDR5 (x12)</td>
<td>16GB HBM2 (x4)</td>
</tr>
</tbody>
</table>

Lower Power per bit transferred

~20 pJ/b → <10 pJ/b

Courtesy of NVIDIA
1st Interposer SIP with HBM

- The 1st Product with HBM (2015)
  - 28nm GPU + 4 HBM1 (4 GB)
  - Large interposer size 1010 mm²
  - 1st non-CoWoS interposer product
  - Different suppliers for interposer and integration (UMC/ASE)
  - Memory bandwidth: 512 GB/s
2nd Generation CoWoS®: Milestones Achieved

- Record-large chip size: 1200 mm² (Si interposer)
- Integrate 3D memory stacks with logic by CoWoS®
- 150B transistors in a package
- Manufacturing infrastructure of 3rd-party dies on CoWoS®
- A number of performance breakthroughs
CoWoS® SIP: Cost vs. Value

• Volume is by far the No.1 factor in the cost equation
  – Not yet find a niche in mobile applications
  – Firm demand in the extremely high-end market (Cloud)

• Interposer is an “add-on” technology
  – High intrinsic cost is unavoidable compared with flip chip

• The key is whether it has sufficient value to justify the cost?
Key Merits of CoWoS® Integration

• **Density:** Sub-micron RDL interconnects
  – Dual damascene, plenty of room for scaling
  – Small via, no routing penalty
  – Fab-class, low defect density

• **Capacity:** Super large interposer
  – 1200 mm² in production
  – Enables highest level of multi-die integration

• **Native to HBM integration**
  – JESD235A compatible. No customization needed.

• **Eliminates ELK related CPI !!!**

• **Same thermal solution as flip chip**

Source: tsmc
Summary

• CoWoS® is an excellent high-end SIP platform
  – High yield, good reliability
  – Market leader since 2012
  – Fast time-to-market
  – Very wide technology envelope

• CoWoS® is a big enabler for HBM
  – Natively compatible with JESD235A
  – Realize the goal of logic-memory integration

• Growing demand that will last for long
  – Extremely high-end cloud and supercomputer systems
  – Highly flexible for heterogeneous integration. E.g., core/IO, memory, SerDes, Si photonics,....
Thank You

Expect Logic-based 3D IC to come out soon