2.5D/3D IC with Si Photonics

Tolga Tekin
Photonic & Plasmonic Systems,
Fraunhofer Institute for Reliability and Microintegration (IZM)
Si Photonics

Applications: (Teledyon, Datacom)

Moore's Law

HISTORY:
- 80s
- nm

Converging Systems:
- Foudries (generic)
- Open capac

PACKAGING

HELLO

PLATON iPHOS RAMPLAS

Phox Trot

IP?

Library? OPEN!!

SiNx?

VS. InP, benefit, active?

> Interfaces

3D TSV

SiP, hetero Si, Integ.

Roadmaps:
- Intel
- Sand, Oracle
- IBM

12M

□ opto PCB

Glass, Ceramic
Technological frontiers between semiconductor technology, packaging, and system design are tending to disappear. Designers of chips, packages, and systems will have to work closer together than ever before in order to drive the performance for future microelectronic systems.

The semiconductor technology is heading the basic physical limits to CMOS scaling. The scaling geometries alone do not ensure improvement of performance, less power, smaller size, and lower cost. It will require “More than Moore” through the tighter integration of system level components at the package level.
Bottleneck

A key bottleneck to the realization of high-performance microelectronic systems, including SiP, is the lack of low-latency, high-bandwidth, and high density off-chip interconnects. Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include the high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to crosstalk.

Obviously, the motivation for the use of photonics to overcome these challenges and leverage low-latency and high-bandwidth communication.

The objective is to develop a CMOS compatible underlying technology to enable next generation photonic layer within the 3D SiP towards converged microsystems.

doi: 10.1109/JSTQE.2011.2113171
Converging Technologies

- Converging technologies are shaping the future of our society. Boarders between disciplines are disappearing.

- Information and communication technology transformed our daily life in last century.

- New technologies such as nanotechnology have significant potential for further transformation. ICT manufacturing concepts, instead of very specialized production lines more and more generic approaches are required to serve a broader area of interest

- Concentrated know-how and the enormous qualified technology base is available from some institutional core-players in the research field of packaging.
In the Age of Converging Technologies

**FACT:** System complexity and functionality are increasing

**TARGET:** Seamless applications (ICT)

**FIRST STEP:** Generic foundry and packaging approaches

- That can be satisfied by heterogeneous integration of different technologies, leading to the best compromise in systems functionality and cost of ownership for higher multi functional converging systems.

- All these technologies need to be optimized

- All these technologies need to be adapted into a modular integrated process flow.
...The Enabling Technology?

**Electronics**

- Electrical interconnects: limited by RC-delay
- Electronics is aspect-ratio limited in speed

\[ R \propto \frac{L}{A} \quad \oplus \quad C \propto L \Rightarrow B_{\text{max}} \propto \frac{1}{RC} \propto \frac{A}{L^2} \]

\[ \Rightarrow B_{\text{max}} \leq 10^{16} \times \frac{A}{L^2} \text{ (bit/s), and } A \ll L^2 \]

..but still the most mature “intelligence platform”
...The Enabling Technology?

**Silicon Photonics**

- Integrated optical components based on Silicon
- Energy-efficient, high bandwidth data communication on short distances
- Bit rate is limited only by the carrier frequency (100Tb/s)

⚠️ **Light propagation**: subjected to **diffraction**

⚠️ **down-limits component size**

Source: AMO

Source: IBM
...The Enabling Technology?

**Plasmonics**

- Propagation of **Surface Plasmon Polariton** (SPP) modes using metallic nanostructures
- EM waves guided at the metal/dielectric interface

- **Sub-wavelength confinement!**
  - No limitations in speed and size
  - Seamless interface between optics-electronics

**Loss**
Combine Benefits On-Chip

Classical vs. plasmonic devices

Electronics - processing, control
Silicon photonics - low-loss passive optics
Plasmonics - low-power active functions

Diffraction limit

10nm 100nm 1μm 10μm 100μm 1mm

RC-delay limit

The next chip-scale technology!!


✓ electronics for “smart functions” (processing, control)
✓ Silicon photonics for low-loss passive optics
✓ Plasmonics for low-power active functions
The Roadmap for Photonics

Network on Chip

Success Stories...

Case 1: Microelectronics ICs

1979: Mead-Conway text was published. Multi project wafer concept enables users to share the cost.

1981: MOSIS was established at the Information Sciences Institute of the USC by DARPA to provide cost-effective advanced IC fabrication.

1985: DARPA & NSF extended the service to US universities.


2005: Interfaces to CMOS processes that support eight layers of metal, resistor and capacitor layers, NPN transistors, and MEMS devices. Mask generation, wafer fabrication, and device packaging are contracted to leading industry vendors.

Aggregation of multiple designs onto one mask set is possible, because of their common building block: Transistor - Every transistor is same
Success Stories…

Case 2 - MEMS

1992: MUMPs was launched in MEMS Technology Applications Center within MCNC (funded by State of North Carolina, DARPA, …).

1999: MEMS business unit spun off into a new company, Cronos Integrated Microsystems Inc.

2000: JDS Uniphase bought Cronos.


MEMS and Nanotechnology Exchange provides expertise in design and fabrication services

Sandia National Laboratories
Success Stories...

Case 3 – Photonics ICs

It is not just electrons, but also photons

There is no such common building block as transistor.

Basic components for PICs:
- Passive waveguides (MMI, s-bend, spot-size conv.)
- Lasers (DFB, DBR, …)
- Semiconductor optical amplifiers (GC-SOA, GS-SOA, …)
- Electro-absorption modulators
- Detectors

with
- Different materials and compositions
- Different doping
- Different photon wavelengths
Quo vadis?

Merging of Silicon Electronics and Photonics

1) Light Source
   - External Cavity Laser Light Source

2) Guide Light
   - Wave-guides
   - Tapers
   - Splitters
   - Switches, Couplers, & others

3) Fast Modulation
   - Silicon Modulator

4) Detect Light
   - Photo-Detector

5) Low Cost Assembly
   - Passive Alignment

6) Intelligence
   - CMOS

BUILDING BLOCKS OF SILICON PHOTONICS by Intel
Silicon Photonics, Packaging and Design Rules for Photonic ICs
Silicon Photonics Activities at Fraunhofer IZM

• ePIXnet
• HELIOS
• PLATON
• iPHOS
• RAMPLAS
• PARADIGM
• UPVLC
• PhoxTroT
• COMANDER
• L3Matrix
Smart Packaging of Silicon Photonics Chip

Fibre-array based interconnection without gloop top

Encapsulated SOI chip on fibre-array in comparison to 1 Euro Cent coin

g-Pack – Generic Packaging for SOI O/E Multiport

Inverted Taper based Coupling for V-Groove Integration

- Adapt to standard layouts for optoelectronics devices
- For passive chip assembly
- Improvement in the alignment
- Anisotropic KOH etching

J. V. Galan et al. “CMOS compatible silicon etched V-grooves integrated with a SOI fiber coupling technique for enhancing fiber-to-chip alignment” IEEE LEOS GFP ThP13 2009
Low Cost Active-Passive & Low Profile Package

Joint development with UPVLC
Design Rules for Si Photonic ICs

Alignment Tolerances of Grating Couplers

- Measured alignment tolerances
- ±1-2 µm: loss < 1 dB

Misalignment Fibers in V-Groove Array
Transmission Test on Smart Packaged SOI Chip

Uniformity: ± 1 dB
Fiber coupling penalty: ~ 1 dB

Fraunhofer IZM’s Approach
Quo vadis?

Merging of Silicon Electronics and Photonics

2) Guide Light

Wave-guides

Tapers

Splitters

Switches, Couplers, & others

5) Low Cost Assembly

6) Intelligence

BUILDING BLOCKS OF SILICON PHOTONICS by Intel
Hetero Silicon Photonics - *Integration Platform*

Targeting high-performance, low-cost, low-energy and small-size components across the entire interconnect hierarchy level can definitely not rely on a single technology platform.

**OBJECTIVE**

Create the optimal synergies between different technologies streamlining their deployment towards Tb/s-scale, high-performance, low-cost and low-energy optical interconnect components and subsystems

“Mix & Match” components / building blocks to deliver the optimal heterogeneous integration and to align their synergistic deployment towards the specific needs of individual functions

Tolga Tekin, Michael Töpper and Herbert Reichl, "PICSiP: new system-in-package technology using a high bandwidth photonic interconnection layer for converged microsystems", Proc. SPIE 7366, 736618 (2009); [http://dx.doi.org/10.1117/12.821690](http://dx.doi.org/10.1117/12.821690)
Silicon Interposer with Optical Layer

adaptation to 3D VSI process flow

Leveraging know-how, experience and technology of 3D heterogeneous integration, including system-in-package

3D wafer-level system integration (300mm wafer)
• Die-to-wafer and wafer-to-wafer bonding
• Wafer-level assembly and 3D stacking
• Evaluation of die-to-wafer (D2W) and wafer-to-wafer (W2W) assembly technologies
• 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (< 50μm)
• 3D IC assembly with thin and ultra-thin chips (20-150μm)
• Through silicon via technology
• TSV diameter: 2 – 20μm; aspect ratio: 5 to 30
• Silicon interposer technology with high-density wiring
• Interposers with high-density Cu-TSV
• High-density multilayer copper wiring (min. 2μm line /space)
• Embedding of active and passive devices into the silicon interposer
• Wafer thinning and handling technology
• Temporary wafer bonding and debonding technology
• Wafer bumping technology
Building-Blocks for Hetero Silicon Photonics

Optical
- Optical waveguides
- Coupling to fiber
- 3dB splitter
- Ring resonators
- MUX/DEMUX
- Switches
- MZI
- ...

Electro-optical
- Photodetectors
- Light sources: LED, VCSEL...
- ...

Electrical
- Through-Silicon Vias (TSV)
- Transmission line: CPW, slotline...
- Antenna
- Heater
- ...

developed in projects...
doi: 10.1109/PHOTONICS.2010.5698810
Buffering as a Generic HPC Problem

- Latency of the entire HPC is limited by the nsec access time of electronic RAM

...but electronic RAM is the only available solution for the HPC Storage Area

http://www.ict-ramplas.eu
Short-Range mmW Very High-Speed Data Link

To develop compact, low power, high performance transceivers that enable wireless data transfer at sub-terahertz carrier wave frequencies based on optical signal generation and processing.

G. Carpintero "Integrated photonic transceivers at sub-terahertz wave range for ultra-wideband wireless communications" EU ICT RF-MST Cluster Workshop 2/07/2012 - Antalya
Integrating RoF with 60GHz wireless and FTTH...  
...in a photonic chip

Design, development and deployment of a fully converged Next-Generation Fiber-Wireless network architecture

Progress & Achievements
@Fraunhofer IZM
Heterogeneous Integration

Silicon Photonics as integration platform
- Designed by IZM
- Fabrication outsider
- Characterized in IZM
- Integrated in IZM

Plasmonics switches
- Designed by SDU
- Fabricated in UB
- Characterized in IZM
- Integrated in IZM

Control IC
- Designed by IZM
- Fabricated outside
- Characterized in IZM
- Integrated in IZM

Fiber-to-Si coupler
MUX
Waveguides
Electrical wiring
Si-to-DLSSP interface
Plasmonic switching elements
Logic IC

PLATON SOI Platform
Building Block: Silicon Waveguide

“First” bunch of chips

- Propagation Loss: 3.5dB/cm
- TM grating couplers > 13dB
- Overall loss > 33dB (2cm Si)

2010

- y = 2.4854x + 29.069
- R² = 0.9907

2013

- y = 2.491x + 28.469
- R² = 0.9519

2x2 PLATON router SOI motherboard

- Propagation Loss: 1.5dB/cm
- TM grating couplers ~ 3.25dB
- Overall loss ~10dB (2cm Si)

- More than 20dB loss reduction
- Record low-loss TM GC

Equation:

\[ y = 2.4854x + 29.069 \]
\[ R^2 = 0.9907 \]

\[ y = 2.491x + 28.469 \]
\[ R^2 = 0.9519 \]
Building Block: Fiber-to-Si coupler

Optimized TM Grating Coupler (IZM)

✓ Grating coupler design (IZM)
✓ SOI waveguide fabrication (AMO)
✓ Characterization (NTUA, AMO, IZM)

Record low losses for TM GC: 3.25dB!!!
Building Block: MUX / DEMUX

Design of the MUX Building Block (IZM)

- Eight stages with 2nd order RRs
- Clustered in two groups with different radii for power efficiency
- Heaters between stages for precise phase control

MUX1: R1=12um; R2=11.7um

MUX2: R1=9um; R2=9.2um
Building Block: Electrical wiring

Fabrication AMO
Assembly & Packaging

✓ Design of package using commercial available components and standard microsystem integration technologies and design rules
  ✓ Multi fiber array
  ✓ Dense connector
The Final Tb/s Router Package

Control IC

SOI motherboard

Plasmonic switch
Data Center / Photonic Interconnects
Global Demand for Digital Information by 2020

- **44ZB**: Amount of data that will be created annually
- **13ZB**: Amount of data that will need to be stored
- **6.5ZB**: Amount of data that installed capacity will be able to hold
- **55%**: Amount of data that will be in the cloud

Source: IDC, Cisco
Main Challenge / Requirement: Cost

Optical interconnect migration down to sub-TOR subsystem level will be gated by transceiver and connectorized link cost.
Building Blocks in the Data Centre

- Data Storage Array
- High Performance Computing and Storage
- Integrated Application Platform
- Storage Server
Increasing Disaggregation in Data Centers

Servers, Racks and Data Centers comprised of modular subsystems which can be broken apart and reassembled to satisfy broad range of ICT requirements.

Higher bandwidth optical connections required between non-localised dispersed modules working together.
Challenge: Adoption of Photonic Interconnect

- Cost
- Power
- Performance
- Applications
- Reliability
- Form Factor
- Trade-off Space
PhoxTroT

PhoxTroT is a European *flagship* research project focusing on
★ high-performance,
★ low-energy,
★ low-cost,
★ small-size

Optical interconnects across the whole data center ecosystem:
★ on-board,
★ board-to-board and
★ rack-to-rack.

http://www.phoxtrot.eu
The PhoxTroT Vision

Terabit/s Optical Interconnect Technologies for On-Board, Board-to-Board, Rack-to-Rack data links
PhoxTroT tackles optical interconnects in a holistic way, synergizing the different technology platforms in order to deploy the optimal "mix&match" technology and tailor this to each interconnect layer.
PhoxTroT - Optical Interconnection Technologies

http://www.phoxtrot.eu
PhoxTroT - Opto-Chips

Increasing optical functionalities

http://www.phoxtrot.eu
TSV serve as enabler for interposers with data exchange between backside and frontside

ams, IZM
Tilted Bonding Process

Stereo microscope picture of VCSEL bonded with 10° angle

Cross section of VCSEL bonded with 10° angle
3D Integration Techniques

Assembly of TIAs and drivers on interposers with Cu pillars

TIAs and drivers are assembled on the TSV side of the interposer. Tools protecting the Cu pillars (and later VCSELs/PDs) on the WG side have been used.

http://www.phoxtrot.eu
3D Integration Techniques

http://www.phoxtrot.eu
Full Process Development

Planar glass waveguide integration → Thin film metallization → Glass laser cutting

Cross-section glass with waveguides

Thin film metallization on glass

Cut-out in glass panel

Embedded glass layer in PCB

200mm wafer-level

fber-to-board

chip-to-board

Assembly optical coupling interfaces → Assembly → Glass embedding and PCB process
Advanced packaging technologies will improve future systems:

1. Packaging determines **functionality, cost and reliability** of future systems.

2. System-in-Package is the **way** for future subsystems.

3. Future systems are very high complex systems and contain different physical functions. Therefore **modularity in heterogeneous integration** is required.

4. Future systems combine optical and ultra high frequency functions. They contain antennas, batteries, sensors, optical components, and microelectronic devices. With this a large variety of materials will be applied. For all these components a **common smart support substrate such as ‘Silicon’** will be of importance for future systems.

**HETERO SILICON PHOTONICS - Integration Platform**