Plasma Dicing: More Die – Stronger Die
Prepared for Semicon Taiwan

Richard Barnett
Etch Product Manager
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Contents

■ FOWLP & Dicing
■ Plasma Dicing
■ Bosch Process (DRIE)
■ Benefits of DRIE for Dicing
■ Integration Schemes & Challenges
■ Die Strength Advantages
■ Die Density Gains
■ Thin Wafer Capability
■ Cost of Ownership Performance
■ Summary
Use of FOWLP is all about flexible integration and lowering cost.
FOWLP & Dicing

Different Process – Same End Product

- Wafer dicing
- Wafer reconstitution
- Molding
- RDL → Singulation
- Bumped Die
- Flip chip bonding
- Molding → Singulation
- FO WLP
- WL – Chip First
- FO CLP
- PL – Chip Last

Plenty of cost saving opportunities with Yield & Throughput improvements before you get to FO
Especially with Plasma Dicing
Plasma Dicing – A new paradigm

- Dicing is not new
  - Using plasma etching for dicing is new
  - Step change in back-end process flows

- Back-end and front-end are not so different
  - Same key objectives;
  - Yield Up and Cost Down

- Disruptive technologies require time to establish themselves
  - “Bringing back-end into the front-end”
  - Discover and overcome roadblocks
  - Gain acceptance & show capability

- The etch technology is available now
  - Integration challenges to be overcome
The “Bosch” Process
- Si etch process
- Repeating loops
  - Polymer dep
  - Polymer removal
  - Isotropic Si etch

There are fundamental considerations for this approach
- Define the Si to be etched
- Provide a compatible etch structure
- Manage test structures and alignment marks – metals & dielectrics
Wafers & Frames

DBG – Dice Before Grind

- ‘Standard’ equipment
- Partial F/S DRIE
- Invert wafer & frame mount
- Singulate during B/S grinding

DAG – Dice After Grind (On Carrier)

- ‘Standard’ equipment
- Temporarily bond to wafer sized carrier
- Singulate during DRIE
- Remount die onto tape/frame for pick & place

DAG – Dice After Grind (On Frame)

- Frame based equipment
- Singulate during DRIE
- Drop-in replacement for conventional dicing

**Frame**
- Plastic or SS
- 296mm OD (6” & 8”); 400mm OD (12”)

**Tape**
- Adhesive + Carrier Film
- PVC, PO, PET

Standard Substrates

Standard Equipment
Consistent, damage free singulation

- No chips, no cracks
- Same sidewall behaviour…wafer-to-wafer
- Repeatable etch performance….ensured with EPD
- Cost of inspection/cost of quality – potential to reduce/eliminate inspections

MEMS 2014 reference
Benefits of DRIE for Dicing
Yield & Cost Benefits

- No Damage
  - Bosch etch creates clean scallops
  - Active cooling to prevent heating
  - No vibrations, debris, water
  - Increased die strength
  - Yield improvement
  - Potential to eliminate inspections
  - Able to cope with thinner wafers (≤50μm)

- Die Density
  - Narrow lanes (<10μm) increase usable Si area
  - Non-orthogonal layouts can be used
  - Crack stop areas can be eliminated

- Throughput
  - Parallel process
  - High Si etch rates
  - Option to use cluster platforms
Integration Considerations

- Die shape, size, area, packing
- Dicing lane width
- Removal of non-Si structures
- Protection of device structures

Layout for Plasma Dicing

Manage Process Flow

Additional Mask Layers, or “Self” Masking

Lane definition by LASER or Blade

Compatible & Defined Dicing Lane
Lane definition by LASER & Blade

- Quality of lane definition not assured
  - Clearing non-Si material from lanes
  - Edges not as “sharp” as photolithography
  - Tuned DRIE can manage this case
  - “Cleans up” top CD of feature

- What if non-Si cannot be removed?
  - E.g. LASER cannot ablate metals
  - OK, if material does not “bridge” lane
  - Etch will simply “go around” the obstruction

- This is most suited to larger die
  - Less affected by t’put of blade/LASER
  - No risk to die strength !!
Metals cannot be etched during plasma dicing

- “Al, Au, Ti, Cu etch with a tape & frame?”
- Ideal case - No dielectric or metals in lanes
- Solder bumps & bondpands are OK

Backside metal can be an advantage

- Clamp to metal
- Access higher t’put process windows

But, how are die separated?

- An additional step is required

Multiple backside metal (BSM) separation options available

- Tape selection is important here
- Dependant upon separation method;
  - Cleaving
  - Stretching
  - Blade/LASER
Other Critical Considerations

■ Tape Choice
  ■ Majority of tapes can be used
  ■ Some perform better than others
  ■ Depends on subsequent steps/process windows
  ■ Reaction of film & adhesive to plasma conditions
  ■ Ensuring no impact on pick/place performance

■ Test Pads
  ■ Lane width reduction to accommodate more die
  ■ Test pads require minimum width for probe heads
  ■ Below minimum width; test pads have to move
    ■ Use a “die” location
    ■ On-die test structures
Die strength is a key attribute, and becoming more critical

Why?

“Harsh” environments are all around us … Especially for IoT !!!
Die strength is a key parameter

- Plasma dicing gives approx 2x gain in die strength
  - Compared to conventional DAG techniques
  - And 20% gain versus Stealth for DBG
- Large notch significantly reduces die strength, even c/w blade
  - <50% of die strength from controlled plasma dicing
  - Notch control is critical for successful plasma dicing
Importance of Process Control

- Etching to tape is similar to SOI
  - Insulating stop layer – in this case a tape
  - Notching die underside at Si/tape interface

- Notching can be prevented
  - Requires EPD & management of bias RF
  - Claritas to enhance OES detection
  - Pulsed bias RF to dissipate charge
Impact of Notch Control
Ability to protect die strength

- Use of Claritas plus pulsed bias gives best notch performance
  - Early detection; of tape minimised and focussed overetch
  - Protect tape and die sidewall from excessive overetch

- More potential impact for smaller die (~1mm² or less)
  - Where notch to die size ratio can be significant

- Large Notch
  - 8~10x scallop size

- Notch ~ Scallops
- Notching <3μm

With EPD
With Overetch control

Without EPD
Without Overetch control

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Die Density & Die Outline

- Reduction in dicing lane width frees up real estate
  - Typically gives biggest gains for smaller die; <1mm²
- Die area can be reduced with removal of crack stop regions
  - Die area reduction of up to 40% may be possible
  - Allowing further consolidation of die layout

![Die Per Wafer vs Dicing Lane Width](image)

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Trends towards thinner wafers

- Device performance, stacking, etc are pushing thinner wafer trends
  - 100-200µm ➔ <50µm

- Conventional dicing techniques begin to pose many difficulties here
  - Throughput restrictions to minimise damage
  - Vibration
  - Heat affected zones
  - Etc

- Plasma dicing is able to cope easily with ultra-thin wafers
  - Higher throughputs as wafer thickness reduces
  - No damage, no heat effects, etc

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Examples of plasma dicing

- Range of integration schemes shown
  - Lithography, LASER definition of lanes, etc
- High dynamic wafer throughputs achieved
  - 3wph for thicker wafers up to 9wph for thinner wafers
Throughput

- Plasma has a distinct advantage as die sizes decrease
  - Number (& distance) of dicing lanes increases
  - And as wafer thickness reduces

![Graph showing Plasma has a distinct advantage as die sizes decrease](image1)

![Graph showing Blade & LASER increase cycle time as die size reduces](image2)

![Graph showing Higher etch rates for thinner wafers](image3)
CoO Comparison

- All things being equal…..
  - On face value, LASER has the higher throughput
  - With lower capital costs than plasma, but what about CoO?

![Graph showing Throughput (wph) for Blade, LASER, and Plasma with assumptions provided.](image)
CoO Comparison

- Take into account...
  - Yield
  - Increased die count per wafer
  - Improved die quality

Utilising benefits of Plasma generates significant CoO advantages over conventional techniques.
Plasma dicing has rapidly become an accepted technique
- Although still in early days of the adoption cycle

Hardware and processes available now
- Based on existing production proven process solutions

Key issue for plasma dicing is integration
- Metals & Dielectrics
- Patterning

Plasma is proven to deliver improved die strength
- Versus blade, LASER and Stealth dicing
- No damage
- Claritas and Bias Pulse Control shown to be critical for DAG
- Minimising notching at tape interface giving higher die strength

Significant CoO benefits moving to Plasma
- Higher yields
- Higher throughputs as wafers get thinner & die get smaller
- Plasma has a major cost per die advantage compared to other techniques