Multi-Chip Embedded Circuit Board, "WABE".

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Outline

• Introduction
  – Demand for Chip Embedded Printed Circuit Board technology

• Fujikura’s Polyimide PCB based IC-chip embedding “WABE Technology®”
  – Fabrication Process
  – Results
  – Reliability

• Multi-Chip embedding technology

• Conclusions
Background & Motivation
Demands for chip embedding technology
Polyimide PCB based IC-chip embedding
“WABE Technology®” - Our Proposal
Motivation for Chip Embedding

Demand for downsizing wiring boards and packages

Double-sided Board  Multi-layer Board

Further reduction in size

Passive embedding  IC-chip embedding

Effective to shrink board footprint and thickness
Another Point of View:

- Integration of the multilayer substrate, the connector, the wiring, and the interposer.
- High density parts mounting with freedom of wiring.
- Exclusion of the plating and etching process from the eco-friendly viewpoint.
WABE Technology®
(Wafer And Board level device Embedded Technology)

Polyimide film (20 ~ 50 μm)
Copper circuit (10 ~ 20 μm)
Conductive paste via

Solder Ball
Thin WLP-IC chip (85 μm)

(1) Ultrathin embedded chip
(2) Flexible multilayer wiring board
(3) Interstitial via hole filled with conductive paste
Example

SMT (3.5 mm x 3.5 mm)

WABE (2.5 mm x 2.5 mm)
1 chip embedded, 4 chips SMT

50% footprint reduction!
WABE Technology®
Fabrication Process & Features
Process Flow of WABE

**Embedded Chip**
- RDL process

**Wiring board**
- FPC manufacturing process

**Co-lamination process**
- Forming RDL
- Back grinding (thinning)
- Singulating
- Forming copper circuits
- Drilling via hole
- Filling with conductive paste

**Backend process**
- SMT, Molding, Bumping, Marking, Singulation
Fabrication Wafer Level Process

Incoming Full Thickness Wafer

Apply and Pattern resin 1 Layer

Plate and Pattern Copper 1 Layer

Apply and Pattern resin 1 Layer

Plate and Pattern Copper 2 Layer

Back Grind to 85 μm
Fabrication Circuit Board Process

**Single Sided**

- Single side CCL
- Photolithography, Cu etching
- Adhesive lamination
- Via hole drilling
- Conductive paste printing
- Conductive paste

**Double Sided**

- Double side CCL
- Laser drilling
- Via plating (Filled, Non-filled)
- Photolithography, Cu etching
- Cavity punching
Fabrication③ Lamination

Stack and Alignment

Unit layer

Embedding IC

1 step lamination

Press and Heat

Adhesive

Conductive paste

Solder Mask, ENIG

SEMICON TAIWAN
Co-lamination method by vacuum hot press with WLP-IC chip

One step lamination!
Backend Process

SMT

Molding, Bumping, Singulation
## Miniaturization Example by WABE Technology®

<table>
<thead>
<tr>
<th>Package Structure/Application</th>
<th>(mm^2)</th>
<th>Original Design</th>
<th>WABE Design</th>
<th>% Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEMS Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X-Y Area</td>
<td>17.7</td>
<td>7.0</td>
<td>60%</td>
<td></td>
</tr>
<tr>
<td>Volume</td>
<td>21.7</td>
<td>7.9</td>
<td>64%</td>
<td></td>
</tr>
<tr>
<td>Power Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X-Y Area</td>
<td>36.0</td>
<td>30.5</td>
<td>15%</td>
<td></td>
</tr>
<tr>
<td>Volume</td>
<td>32.4</td>
<td>9.6</td>
<td>70%</td>
<td></td>
</tr>
<tr>
<td>Control Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X-Y Area</td>
<td>22.3</td>
<td>16.5</td>
<td>26%</td>
<td></td>
</tr>
<tr>
<td>Volume</td>
<td>54.7</td>
<td>20.3</td>
<td>63%</td>
<td></td>
</tr>
<tr>
<td>Control Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X-Y Area</td>
<td>16.0</td>
<td>7.3</td>
<td>54%</td>
<td></td>
</tr>
<tr>
<td>Volume</td>
<td>16.0</td>
<td>7.5</td>
<td>53%</td>
<td></td>
</tr>
</tbody>
</table>
Multi-chip stack embedding
More Miniaturization by Multi-chip embedding

Surface; 3 chips

Surface; 1 chip Embedded; 2 chips

Surface; 1 chip Embedded; 2 chips

Area 100%

56%

33%

Multi Chip Stack embedding technology
Fabrication

Intermediate Layer

- Insulating film
- Polyimide
- Adhesive lamination
- Adhesive
- Through hole drilling
- Via hole
- Conductive paste printing
- Conductive paste

This intermediate layer enables multi-chip embedding by co-lamination process
Fabrication⑤ One Step Co-lamination Process

1. Co-lamination

2. Press and curing

Complex Structure produced by Simple Process!
Actual Result

Standard WABE package (Cross section)

chip-stack
## Comparison of chip-embedding Technologies

<table>
<thead>
<tr>
<th>Process flow</th>
<th>WABE technology</th>
<th>Conventional</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simple</td>
<td>Complex</td>
</tr>
<tr>
<td></td>
<td>One step lamination process</td>
<td>Build-up process</td>
</tr>
<tr>
<td>Cycle time</td>
<td>Short</td>
<td>Long</td>
</tr>
<tr>
<td></td>
<td>Parallel FPC fabrication</td>
<td>Sequential process</td>
</tr>
<tr>
<td>Die Losses</td>
<td>Minimum</td>
<td>Multilayer board fabrication process after embedding</td>
</tr>
<tr>
<td></td>
<td>Use of known good die and known good circuit</td>
<td></td>
</tr>
<tr>
<td>Via density of embedding layer</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td></td>
<td>Fully stacked IVHs for any layer</td>
<td>Core and buildup layer</td>
</tr>
<tr>
<td>Multi chip-stack embedding</td>
<td>Easy</td>
<td>Difficult</td>
</tr>
<tr>
<td></td>
<td>Almost same as one-chip</td>
<td>Build-up process</td>
</tr>
</tbody>
</table>

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![Image: Comparison of chip-embedding Technologies diagram]
Multi-chip stack embedding WABE
Result reliability
Evaluation Embedded Two EEPROMs

<table>
<thead>
<tr>
<th>Item</th>
<th>dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu layers</td>
<td>7 layers</td>
</tr>
<tr>
<td>dimension</td>
<td>4.4 x 3.0 mm, <strong>0.4 mmt</strong></td>
</tr>
<tr>
<td>embedded chips</td>
<td>3.5 x 2.0 mm, 0.085 mmt</td>
</tr>
<tr>
<td>via dia.</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>L/S</td>
<td>50 μm/50 μm</td>
</tr>
</tbody>
</table>

X-section (area of embedded chips)
Component Level Test

preconditioning: MSL3 (30°C/60%RH, 192hr, 3times reflow)

<table>
<thead>
<tr>
<th>Test</th>
<th>Condition</th>
<th>n</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>temperature cycle test</td>
<td>-40°C ↔ 125°C, 1hr/cyc, 500cyc</td>
<td>45</td>
<td>PASSED</td>
</tr>
<tr>
<td>temperature humidity bias test</td>
<td>85°C/85%RH, 500hr</td>
<td>45</td>
<td>PASSED</td>
</tr>
<tr>
<td>high temperature storage test</td>
<td>105°C, 1000hr</td>
<td>45</td>
<td>PASSED</td>
</tr>
<tr>
<td>unbiased highly accelerated stress test</td>
<td>130°C/85%RH/230kPa, 336hr</td>
<td>45</td>
<td>PASSED</td>
</tr>
</tbody>
</table>
# Board Level Test

preconditioning: MSL3 (30°C/60%RH, 192hr, 3times reflow)

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<td>16</td>
<td>PASSED</td>
</tr>
<tr>
<td>temperature humidity bias test</td>
<td>85°C/85%RH, 2.6V&lt;sub&gt;DC&lt;/sub&gt;, 500hr</td>
<td>12</td>
<td>PASSED</td>
</tr>
<tr>
<td>high temperature storage test</td>
<td>85°C, 2.6V&lt;sub&gt;DC&lt;/sub&gt;, 500hr</td>
<td>12</td>
<td>PASSED</td>
</tr>
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</table>

All the tests passed with no failure
Polyimide PCB based chip embedding “WABE Technology®”

- by simple one step co-lamination process
- as thin as 0.4 mm, including 2 embedded IC-chips
- reliability verified

Ready to shrink your products!
Thank you

Basic

Side by Side

2Chips Stack

3Chips Stack

1chip → 2chips → 3chips