Low Power is Everywhere: Industry Design Trends

The Power of $\mathcal{X}$

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Agenda

- Low Power Design Trends
- Synopsys Low Power Implementation Overview
Low Power is Everywhere!
Design for Power Extends Beyond Mobile Applications

Wireless/Portable
Key Driver: Extend Battery Life

Servers/Networking
Key Driver: Reduce Energy Cost

Cores
Key Driver: End Market Integration

Multimedia
Key Driver: Increase Energy Efficiency

Green initiatives are the primary drivers!
# Evolution of Low Power Design

*Intertwined with Increasing Design Complexity*

<table>
<thead>
<tr>
<th>Mobile Applications</th>
<th>90nm</th>
<th>65nm</th>
<th>45/40nm</th>
<th>32/28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>3M Instances</td>
<td>5M Instances</td>
<td>10M Instances</td>
<td>10M Instances</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>300MHz</td>
<td>550MHz</td>
<td>850MHz-1.5GHz</td>
<td>875MHz-1.5GHz</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>100mW – 1W</td>
<td>100mW – 1W</td>
<td>100mW – 1W</td>
<td>100mW – 1W</td>
</tr>
<tr>
<td><strong>LP Techniques</strong></td>
<td>• Clock Gating/CTS • 1-2 Domains • Power Gating • Multi-Vt • Back-Bias</td>
<td>• Clock Gating/CTS • 3 Domains • Power Gating • Multi-Vt • Back-Bias • Hierarchical</td>
<td>• Clock Gating/CTS • 5-10+ Domains • Power Gating • Multi-Vt • Body Bias • Hierarchical • Channel Length Variations • DVFS</td>
<td>• Clock Gating/CTS • 7-25+ Domains • Power Gating • Multi-Vt • Hierarchical • Channel Length Variations • DVFS</td>
</tr>
</tbody>
</table>

*Source: Synopsys Global User Surveys, 2011*
Designs Continue to Get More Complex

30% of Designs >10 Clock Domains and >3 Voltage Domains

Median Clock Domains Current Design = 6

Median Voltage Domains Current Design = 3

N = 827

N = 758
Power Management is Now the #2 Top Design Challenge

Top Design Challenge(s)

- Timing closure: 48%
- Power management: 39%
- Meeting timing and area goals: 34%
- Tapeout on schedule: 33%
- Power estimation at the Architect/RT level: 21%
- Generation and validation of constraints/exceptions: 14%
- Analog/mixed-signal implementation: 13%
- IP integration: 12%
- Signal integrity: 11%
- IR drop: 10%
- Reducing time for sign-off physical verification: 9%
- Implementing ECOs: 9%
- Increasing yield: 7%
- Equivalence checking: 6%
- Meeting manufacturing test goals: 4%
- Other: 2%

N = 653

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LP Implementation is the #1 Power Challenge for Designers

Power Management Tasks that Present the Greatest Challenge(s)

- Implementation of low power techniques, 36%
- Functional verification of low power behavior, 20%
- Specification of low power intent, 8%
- Post-synthesis power analysis, 26%
- Equivalence checking, 5%
- IP configuration/integration, 4%

2009:

- Implementation of low power techniques, 47%
- Functional verification of low power behavior, 20%
- Specification of low power intent, 7%
- Post-synthesis power analysis, 9%
- Equivalence checking, 5%
- IP configuration/integration, 4%

2010:

- Implementation of low power techniques, 51%
- Functional verification of low power behavior, 11%
- Specification of low power intent, 7%
- Post-synthesis power analysis, 6%
- Equivalence checking, 5%
- IP configuration/integration, 4%

2011:

- Implementation of low power techniques, 51%
- Functional verification of low power behavior, 11%
- Specification of low power intent, 7%
- Post-synthesis power analysis, 6%
- Equivalence checking, 5%
- IP configuration/integration, 4%


N = 283
Usage of UPF Power Intent is Now Mainstream

*Source: Synopsys, Inc. Global User Survey, 2011*
Low Power is Everywhere!

Low Power Techniques Used Across Market Applications

Interpret as: 17% of respondents having “Personal Computing & Peripherals” as primary application use “Low Vdd Standby” low power design technique.

* Percentages equal >100% because multiple answers accepted

Key Components of Low Power Design

- Optimization Engines
  - Galaxy
  - Design Compiler
- Power vs. Complexity
- Low Power Architectural Techniques
- Process
- Power vs. Performance
- Schedule and Quality of Results
Process Determines Power and Performance Baseline

**Options**
- Low Power Process
- Vt Variants
- Standard Cell Architecture

**Selection criteria**
- Design budgets
- Process costs
- IP availability

<table>
<thead>
<tr>
<th>28nm Architecture</th>
<th>High-Density</th>
<th>High-Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>9.5 grids (95nm)</td>
<td>12.5 grids (125nm)</td>
</tr>
<tr>
<td>Raw Gate Density**</td>
<td>3120K gates/mm²</td>
<td>2520K gates/mm²</td>
</tr>
</tbody>
</table>

**Post-shrink on silicon, 60% NAND2, 40% DFF**

*Source: Synopsys*
Architectural Techniques Determine Achievable Power Savings

Effectiveness of Power Saving Techniques Can Change with Each Node

<table>
<thead>
<tr>
<th>Methodology</th>
<th>65nm</th>
<th>45/40nm</th>
<th>32/28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple Voltage Islands</td>
<td>1.2 – 2.5X</td>
<td>1.2 – 2.5X</td>
<td>1.2 – 2.5X</td>
</tr>
<tr>
<td>Multi-Voltage Supplies (MV)</td>
<td>1.3X</td>
<td>1.3 – 1.5X</td>
<td>1.3 – 2X</td>
</tr>
<tr>
<td>Lower VDD Operation</td>
<td>1.3 – 2X</td>
<td>1.3 – 2X</td>
<td>3 - 5X</td>
</tr>
<tr>
<td>MT-CMOS Power Gating</td>
<td>30 - 120X</td>
<td>30 - 120X</td>
<td>30 - 120X</td>
</tr>
<tr>
<td>Biasing: Standby/Body</td>
<td>1.3 - 2X / 2X</td>
<td>1.15 / 1.3X</td>
<td>1.02 / NA</td>
</tr>
<tr>
<td>Multi-Vt Optimization (Leakage)</td>
<td>2 - 5X</td>
<td>2 - 5X</td>
<td>2 - 5X</td>
</tr>
<tr>
<td>Clock Gating</td>
<td>1.3 – 2X</td>
<td>1.3 – 2X</td>
<td>1.3 – 2X</td>
</tr>
<tr>
<td>Clock Tree Synthesis</td>
<td>1.4 – 3.3X</td>
<td>1.4 – 3.3X</td>
<td>1.4 – 3.3X</td>
</tr>
<tr>
<td>Channel Length (Multi-Channel)</td>
<td>NA</td>
<td>3 - 5X</td>
<td>2 - 6X</td>
</tr>
<tr>
<td>DVFS AVS</td>
<td>NA</td>
<td>1.4X</td>
<td>1.4 - 2X</td>
</tr>
</tbody>
</table>

Tradeoff Power vs. Design Complexity
Galaxy Implementation Platform Delivers Predictability

- Comprehensive Multi-Voltage flow with consistent interpretation of power intent
- Built-in power network synthesis
- High accuracy in-design rail analysis
- Concurrent timing, area, power and test optimization throughout
- Optimal usage of Low-Vt cells
- Comprehensive power-aware formal and static verification
# Power Saving Techniques

<table>
<thead>
<tr>
<th>Dynamic Power</th>
<th>Leakage Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Advanced Clock Gating</td>
<td>• Multi-threshold (Multi-Vt) libraries</td>
</tr>
<tr>
<td>• CTS</td>
<td>• Limiting usage of LVt cells</td>
</tr>
<tr>
<td>• Multi-Bit Registers</td>
<td>• Multi-Corner, Multi-Mode (MCMM)</td>
</tr>
<tr>
<td>• Multi-Voltage supplies and shutdown domains</td>
<td>• Biasing</td>
</tr>
<tr>
<td>• Lower VDD operation</td>
<td>• Multi-Voltage supplies and shutdown with state retention support</td>
</tr>
<tr>
<td>• DVFS/AVS</td>
<td>• Channel length cell variants</td>
</tr>
<tr>
<td></td>
<td>• Final-stage leakage recovery</td>
</tr>
</tbody>
</table>
Multi-bit Register for Reduced Power

• Benefits
  – Lower power consumption
  – Smaller area and delay

• Challenges
  – Knowing which registers to bank and replace with multi-bit equivalents - requires timing, connectivity and physical knowledge
Fine Grain Control Over Leakage Optimization

**Single Pass Multi-Vt Leakage**

- 20-70% Lower Leakage

**MCMM Optimization**

- Concurrent
- Sequential
- Time

**Limit %LVt Cell Usage**

<table>
<thead>
<tr>
<th>Leakage Opt</th>
<th>ICC (%Vt)</th>
<th>WNS (ps)</th>
<th>Cell Area</th>
<th>Leakage (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>100%</td>
<td>-124</td>
<td>3.47M</td>
<td>50.88</td>
</tr>
<tr>
<td>%LVt = 20%</td>
<td>19%</td>
<td>-363</td>
<td>3.49M</td>
<td>46.00</td>
</tr>
</tbody>
</table>

**Final Stage Leakage Recovery**

- WN5 = 0.24ns, TN5 = 10.35ns, Leakage = 1.05mW
- WN5 = 0.24ns, TN5 = 16.25ns, Leakage = 0.90mW

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Multi-Corner, Multi-Mode (MCMM) Throughout for Better QoR, Faster

- Reduced iterations between synthesis and place and route optimizations for faster convergence
- Optimize worst case leakage and timing corners, simultaneously
- Common set up for multi-scenario definition
- Signoff compatible with DMSA (Distributed Multi-Scenario Analysis)
Leakage vs. Performance Tradeoff

Channel Length Variation at 40nm

Increasing channel length with lower Vt can be beneficial

Source: Synopsys
IC Compiler Final-Stage Leakage Recovery

- Powerful leakage optimization
  - Architected for multiple channel-length-biased leakage variants and Vt libraries

- Use on final-stage netlist for leakage recovery
  - Reduces leakage power while preserving timing/DRC
  - Minimal physical impact
    - Footprint based

- Complements leakage optimization throughout P&R
Comprehensive Synopsys Multi-Voltage (MV) Flow

- Power Intent Generation, Visualization and Implementation
- Power Network Synthesis with Shutdown
- MV-Aware Placement and Hierarchical Support
- Power-Aware Test
- Power-Aware Static Verification
- Power Analysis
Synopsys Advanced Low Power Solution is Proven

News Release

Industry Leaders Achieve Significant Power and Performance Gains with Synopsys’ Low Power Solution
Advanced Solution Now in Mainstream Usage with More Than 125 Successful Tapeouts

Dec 5, 2011

MOUNTAIN VIEW, Calif., Dec. 5, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that industry leaders worldwide have broadly deployed and successfully taped out more than 125 advanced multi-voltage designs using the Galaxy™ Implementation Platform low power solution and IEEE-1801 Unified Power Format (UPF) resulting in significant productivity, power and chip performance gains. Among these companies are Aquantia, Chongqing Chongyou Information Technology Co., Ltd. (CYIT), Emulex, HiSilicon Technologies, Lantiq, LSI Corporation, Microchip Technology, Movidius, Oticon, Progate Group Corporation, Samsung, Sunplus Technology, TSMC, VeriSilicon, Vimicro and others, targeting a broad spectrum of application markets including consumer electronics, wireless, DSP, mobile, microprocessor, networking, storage and portable medical devices.
Continued Investment in Low Power Implementation

Proven 15 year track record on delivering low power innovation!