Perspectives of Memory Challenges From Equipment Supplier

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Mobility and Internet of Things Are Driving Semi Industry

Mobile market size and growth most significant driver of semi technology and capacity spending

Internet of Things creating new requirements and opportunities for widespread adoption

Electronics Growth

Mobility/cloud driving growth of ~6% - 7%

<table>
<thead>
<tr>
<th>Year</th>
<th>Growth Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2012</td>
<td>2.0%</td>
</tr>
<tr>
<td>2013</td>
<td>2.5%</td>
</tr>
<tr>
<td>2014F</td>
<td>7.0%</td>
</tr>
<tr>
<td>2016/17F</td>
<td>6.0%</td>
</tr>
</tbody>
</table>
Semiconductor Supply Required to Meet Electronics Demand

**NAND Flash**
- Bit growth 35% - 40% per year through 2017
- Solid-state storage driven by mobile and cloud

**Mobile DRAM**
- Mobile DRAM bit growth CAGR of >50% 2013-2017
- Low-power designs require larger die
- Mobile bits > PC in 2014

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**Industry NAND Demand Average**

[Graph showing Industry NAND Demand Average with data points for 2011, 2013, 2015E, 2017E]

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**Mobile DRAM Demand Average**

[Graph showing Mobile DRAM Demand Average with data points for 2011, 2013, 2015E, 2017E]

Source: Gartner, Lam Research estimates
Memory Technology Trends

- Emerging Memory technologies: ReRAM (for NAND), PCRAM, SST-RAM (for DRAM)... each are difficult
- Strong interest in vertical architectures

- Multiple Patterning
  - Litho-Only
  - Double Patterning
  - Quadruple Patterning

- 3D NAND
  - Planar NAND
  - 3D NAND

- Through-Silicon Via
  - Wire-Bond Stacked Chip
  - Through-Silicon Via

- 3-4 steps (mid-D2x)
- 15-20 steps (~D20 nm)
- 30-40 steps (D1x nm)

- Samsung in production
- Others following, but also working on planar

Market adoption:
- CMOS image sensors
- Future growth from memory and logic adoption
Equipment Required to Have Stringent Control of Variability

Need exact copies every time

Microchip

Array of devices

Single devices
Why Variability Control Is Necessary

Tight variability required for higher yields, lower power consumption, improved device performance.
Variability Challenge Is Extraordinary

**Variation Tolerance**
(Example for Critical Dimensions)

- **130 nm Node**: ~10 nm, ~140 atomic layers
- **65 nm Node**: ~5 nm, ~60 atomic layers
- **20 nm Node**: ~1 nm, ~14 atomic layers
- **10 nm Node**: <0.5 nm, ~3-4 atomic layers

Tool differentiation needed to control variability down to atomic scale

Atomic layers based on silicon
# Sources and Approaches to Process Variation

## Microscopic Uniformity
- **Surface Roughness**
- **Pattern dependent variations**

## Across-the-Wafer
- **Radial and azimuthal components**
- **Far Edge Exclusion**

## Wafer-to-Wafer
- **Hardware variability x process sensitivity**

### Approach:
- **RF Pulsing/ IEDF**
- **ALE and ALD**

### Approach:
- **Symmetric tool designs**
- **Tuning knobs for chemical and electrical gradients**

### Approach:
- **Hardware variability reduction (static and dynamic)**
- **Chamber subsystem diagnostics**
PATTERNING CHALLENGE
Critical Passes in Each Patterning Step

Cumulative # critical passes per patterning step:

<table>
<thead>
<tr>
<th>Step</th>
<th># Lam Passes/Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch</td>
<td>1</td>
</tr>
<tr>
<td>Deposition</td>
<td></td>
</tr>
<tr>
<td>Clean</td>
<td></td>
</tr>
</tbody>
</table>

Litho Only
Critical Passes in Each Patterning Step

Double Patterning (DPT)

Cumulative # critical passes per patterning step: **DPT**

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<th>Step</th>
<th># Lam Passes/Step</th>
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<tbody>
<tr>
<td>Etch</td>
<td>1</td>
</tr>
<tr>
<td>Deposition</td>
<td>1</td>
</tr>
<tr>
<td>Clean</td>
<td></td>
</tr>
</tbody>
</table>

# Critical Dimensions
**Critical Passes in Each Patterning Step**

<table>
<thead>
<tr>
<th>Step</th>
<th># Lam</th>
<th>Passes/Step</th>
<th>QPT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch</td>
<td>1</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Deposition</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Clean</td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

*Cumulative # critical passes per patterning step:*

*Quadruple Patterning (QPT)*

Etch, Deposition, and Clean address >2/3 of all multiple patterning critical passes
Variability Control Challenges for Patterning

- **Deposition**: Non-conformal deposition
- **Etch**: Varying widths
- **Clean**: Collapse, Damage
Solutions for Critical Steps in Patterning

**Deosition**
- High conformity ALD film
- Productivity advantage

**Etch**
- Die-by-die uniformity control
- Compensates for lithography

**Clean**
- No pattern collapse
- Productivity competitiveness

VECTOR® ALD Oxide

2300® Kiyo® Family with Hydra™

Next-Generation Spin Clean
Etch Solution Offers Die-by-Die Variability Control

Variability inevitable for incoming wafer

Pre-etch CD variation: ~2 nm

wide variation

CD = critical dimension
Etch Solution Offers Die-by-Die Variability Control

Pre-etch CD variation: ~2 nm

After etch: <0.5 nm

>50% reduction
Unparalleled variability control, improves incoming lithography variation
3D NAND CHALLENGE
Key Process Steps in 3D NAND

- Etch and deposition processes:
  - Stack deposition
  - Channel etch
  - Wordline deposition
  - Slit etch
  - Stair etch
  - Contact tungsten fill
  - High aspect ratio mask open
  - Hardmask deposition
  - Bitline copper fill
  - Dielectric ALD liners
  - Contact etch

Most critical to memory cell formation
Variability Control Challenges for 3D NAND

Stack

- Wavy, not uniform layers

Channel

- Holes not vertical

Wordline

- Voids in metal
Lam’s New Systems for Critical Steps in 3D NAND

**Dielectric Deposition**
- VECTOR® Q Strata™
- Stack

**Dielectric Etch**
- 2300® Flex™ F Series
- Channel

**Metal Deposition**
- ALTUS® Max ICEFill™
- Wordline

- Ultra-smooth, uniform films
- Industry-leading productivity

- High aspect ratios with tightly controlled etch profile
- Proprietary high ion energy source with pulsing

- Void-free tungsten fill
- Inside-out fill process using atomic layer deposition
EMERGING MEMORY CHALLENGES
Numerous RRAM Candidate Materials

Dielectric Material

Electrode Material
## Challenge for Emerging Memory: Non-volatile Etch Materials

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Materials</th>
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<tbody>
<tr>
<td><strong>MRAM</strong></td>
<td>- Electrode: Ru, Ta, TiN&lt;br&gt;- Magnetic: CoFe, NiFe, CoFeB, PtMn, IrMn, Ru&lt;br&gt;- Dielectric: Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;, MgO, NiO</td>
</tr>
<tr>
<td><strong>RRAM / CBHAM</strong></td>
<td>- Electrode: W/ Ag/ Cu/ Co/ Mo/TaSN&lt;br&gt;- Electrolyte: (Ag-Ge-S/ Cu-Ge-S)&lt;br&gt;- Dielectric: Perovskite (CaTiO&lt;sub&gt;3&lt;/sub&gt;, PrCAMnO&lt;sub&gt;3&lt;/sub&gt;, Transition metal Ox</td>
</tr>
<tr>
<td><strong>FeRAM</strong></td>
<td>- Dielectric: PZT (PbZr&lt;sub&gt;1-x&lt;/sub&gt;TixO&lt;sub&gt;3&lt;/sub&gt;): Y1 ((SrBiTa)O&lt;sub&gt;3&lt;/sub&gt;)&lt;br&gt;- Electrode Pt/Ir</td>
</tr>
<tr>
<td><strong>Phase Change Memory (PCM)</strong></td>
<td>- Chalcogenide (Ge&lt;sub&gt;2&lt;/sub&gt;Sb&lt;sub&gt;2&lt;/sub&gt;Te, InSbTe)</td>
</tr>
<tr>
<td><strong>3D-NAND</strong></td>
<td>- Traditional materials&lt;br&gt;- Dielectric: High-k</td>
</tr>
<tr>
<td><strong>DRAM</strong></td>
<td>- Traditional materials&lt;br&gt;- Dielectric fill: ZrO/ AlO/ SrTiO</td>
</tr>
<tr>
<td><strong>(FBC) on SOI structures</strong></td>
<td>- Traditional materials&lt;br&gt;- Dielectric: High-k</td>
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**Non-volatile etch**

Difficult to etch materials are a barrier to scaling.
STT-MRAM Process Challenges

**Challenges**

- **Deposition:**
  - Hermetic seal for encapsulation
  - High-conformality barrier and no void fill at low T < 300°C

- **MTJ Etch:**
  - Vertical profile with no sidewall damage
  - Productive MTBC

- **Clean:**
  - Non-oxidizing MTJ stack
  - Sidewall residue

**Key Requirements**
Vertical profile requires volatile etch by-products

- Tapered profile limits feature scaling

Redeposition of sputter products results in tapered profile in a conventional etcher

\[ \frac{\Gamma_{\text{Neutral}}}{\Gamma_{\text{Ion}}} = 0 \]

\[ \frac{\Gamma_{\text{Neutral}}}{\Gamma_{\text{Ion}}} = 5 \]

\[ \frac{\Gamma_{\text{Neutral}}}{\Gamma_{\text{Ion}}} = 10 \]

Increasing chemical etchant flux
Metallic Etch Rates with Different Compounds

- Challenges
  - Multiple chemistries required to etch the various elements in a MRAM stack
  - Stack composition changing frequently

Source: Lam-University collaboration
Higher Etch Rates with novel etch approach (MMP)

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- Multiple chemistries required to etch the various elements in a MRAM stack
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