CMP Redefined

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Moore’s Law has dominated the CMOS industry for >40 years
- Not affected by cycles, markets, analysts, or the economy

Photolithography and CMP are two critical process technologies that enabled Moore’s Law to continue its trend
- Photolithography enables shrinks
- CMP enables Photolithography

Trend still holds for certain industry segments, but many companies are choosing to pursue other paths to meet their device objectives
• **Segment I – The most advanced, leading edge devices**
  – Wafer sizes: 300mm & possibly 450mm (future)
  – Technology nodes: 65nm, 45nm, 32nm and below
  – Materials: high k, metal gates, ULK, Cu, TSV, etc.

• **Segment II – Improvements to mainstream ICs**
  – Wafer sizes: 200mm & 150mm
  – Technology nodes: 90nm to 350nm and above
  – Materials: oxides, tungsten, STI, etc.

• **Segment III – Emerging technologies & new applications**
  – Wafer sizes: 200mm, 150mm, 100mm and smaller
  – Technology nodes: various
  – Materials: wide range of metals, oxides, polymers, and more
  – MEMS, nanotechnology, SiC, GaN, AlN, SiGe, poly, optics, etc.
## Financial Factors and Trends Across Industry Segments

<table>
<thead>
<tr>
<th>Financial Factor</th>
<th>&quot;More Moore&quot;</th>
<th>&quot;More Than Moore&quot;</th>
<th>Emerging</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Level</td>
<td>Trend</td>
<td>Level</td>
</tr>
<tr>
<td>Average Annual Capital</td>
<td>High</td>
<td>↑</td>
<td>Moderate</td>
</tr>
<tr>
<td>Technology R&amp;D</td>
<td>High</td>
<td>↑</td>
<td>Moderate</td>
</tr>
<tr>
<td>Manufacturing Cost/chip</td>
<td>High</td>
<td>↓</td>
<td>Moderate</td>
</tr>
<tr>
<td>Volume</td>
<td>High</td>
<td>-</td>
<td>High</td>
</tr>
<tr>
<td>Average Selling Price (ASP)</td>
<td>High</td>
<td>↓</td>
<td>Low</td>
</tr>
</tbody>
</table>
The original technology drivers for CMP were (and often continue to be) related to topography issues in other process modules or with the overall process integration.

- **Oxide CMP**
  - Depth of focus at photolithography
    - Worse as linewidths shrank below 0.35 um
    - Worse with additive topography of MLM
  - Metal step coverage
    - Metal thinning on steep sidewalls
    - Topography induced etch effects
    - Inconsistent line resistance

- **Shallow Trench Isolation CMP**
  - LOCOS isolation hit physical limits
  - Shrinks below 0.35 um required new isolation
  - Original integration used reverse mask etch
    - Very sensitive alignment
    - Very expensive due to number of process steps
  - Direct STI CMP required years of slurry innovation and process development

- **Tungsten CMP**
  - Replaces plasma etchback
  - Solves severe plug recess from overetch
  - Lowers defectivity
  - Improves yield
  - Enables stacked vias

- **Copper CMP**
  - Driven by lack of acceptable Cu metal etch
  - Early difficulties with electroplating profiles
  - Cu/barrier metal forms electrochemical cell
  - Introduction of low-k dielectric complicates an already difficult materials system
Each new material or new integration usually requires a new CMP process …. or at least a puzzle to be put together.
CMP Complexity

- **Wafer / Materials Parameters**
  - Size / Shape / Flatness
  - Film Stack Composition
    - Metals (Al, Cu, W, Pt, etc.)
    - Oxide (TEOS, PSG, BPSG, etc.)
    - Other (polysilicon, low-k polymers, etc.)
  - Film Quality Issues
    - Stress (compressive or tensile)
    - Inclusions and other defects
    - Doping or contaminant levels
  - Final Surface Requirements
    - Ultralow surface roughness
    - Extreme planarization, esp. Copper
    - Low defectivity at <0.12 um defect size

- **Pad Issues**
  - Materials (polyurethane, felt, foam, etc.)
  - Properties must be chosen for the job
  - Conditioning method often not optimized
  - Lot-to-lot consistency

- **Slurry Issues**
  - Chemistry optimization often required
  - Mixing and associated inconsistency
  - Shelf life and pot life sometimes very short
  - Slurry distribution system (design, cost, upkeep)
    - Agglomeration and gel formation
    - Filtration is often required
  - Cleaning method specific to slurry and film
  - Waste disposal and local regulations

- **Process Issues**
  - Long list of significant input variables
    - Downforce
    - Platen speed
    - Carrier speed
    - Slurry flow
    - Conditioning method
      - Disk used (material, diamond size, spacing, etc)
      - Force
      - Speed
      - Sweep profile
  - Highly sensitive to local pattern variation
  - Must maintain consistency at high throughput
  - Must optimize for variation of incoming films

- **Integration Issues**
  - Materials Compatibility
    - Electrochemical interactions with two or more metals
    - Film integrity and delamination, esp. low-k
    - Film stack compressibility
  - Interactions with adjacent process modules
    - Photolithography
    - Metal deposition and metal etch
    - Dielectric deposition and etch
  - Electrical design interactions
    - Feature size constraints
    - Interactions with local pattern density
    - Line resistance variation, esp. damascene copper
    - Dielectric thickness variation
    - Contact resistance variation

**Process development teams must balance complexity, cost, risk, and timelines.**
A few common themes run across all segments:
- Device reliability can not be compromised.
- Quality and consistency are very important.
- Cost is almost always a factor, though sometimes not the most important factor.

The rest of the answers depend on which industry segment you are focused on at the time.
Decision Drivers

<table>
<thead>
<tr>
<th>Segment I</th>
<th>Speedsters</th>
<th>More Moore</th>
</tr>
</thead>
<tbody>
<tr>
<td>EQUIPMENT</td>
<td>Willing to buy for new fabs or to retool existing fabs. Drive improvements in both capability and productivity.</td>
<td></td>
</tr>
<tr>
<td>CONSUMABLES</td>
<td>Push performance in nearly every aspect of CMP. Defectivity is becoming an increasing focus.</td>
<td></td>
</tr>
<tr>
<td>MATERIALS</td>
<td>Adapt existing materials whenever feasible, but will not hesitate to integrate new materials when necessary</td>
<td></td>
</tr>
</tbody>
</table>

Summary

- Typical companies: microprocessor and memory makers, large-scale foundries.
- Willing to spend on new fab construction (mostly 300 mm and possibly 450 mm).
- Willing to adapt new materials or processes as needed to achieve performance.
- Designs AND process technology both change at a rapid pace.
- Design focus = performance.
- Process focus = speed and acceptable yield.

Outlook

- Extremely low defect levels at insanely small sizes.
- Topography control to better than 3nm for some levels.
- Reduce wafer-to-wafer variation.
- CMP and cleans for new materials to solve tough physics challenges at sub-32nm design rules.
- Tunable consumables that allow integration teams flexibility to alter rates and selectivities.
- Only a small number of companies are still in this game, but wafer volumes are high at each one.
### Decision Drivers

#### Segment II

<table>
<thead>
<tr>
<th>New Mainstream</th>
<th>Moore than Moore</th>
</tr>
</thead>
</table>
| **EQUIPMENT**  
Preserve capital and extend depreciated tools whenever possible  
Buy tools only for "must have" capacity expansions  
Generally staying focused on 200mm and below |                  |
| **CONSUMABLES**  
Extreme focus on reducing cost per wafer  
Defectivity and other factors to improve yield are also key |                  |
| **MATERIALS**  
Adapt proven materials and process methods ? period.  
Optimize process flows for simplicity and yield |                  |

### Summary
- Wide range of products including digital, analog, mixed signal, power, etc.
- Adapting to a world of flat or falling ASP’s
- Cost factors and yield are generally MUCH more important than technology factors
- Some devices enjoy long lifecycles
- Designs may change rapidly, but process technology intentionally being held much more stable
- Design focus = features and simplicity
- Process focus = cost and maximizing yield

### Outlook
- Reduce cost per wafer polished.
- Lower defects (but only when it improves yield).
- Stable or incremental improvements in performance.
- New product families are generally based on same or similar process flow in existing fabs.
- Adapt existing equipment first, whenever possible, to avoid buying new tools.
- Large broad base of users, but conversion to a new consumable requires justification (ROI).
## Decision Drivers

### Segment III - Emerging Technology

<table>
<thead>
<tr>
<th>EQUIPMENT</th>
<th>CONSUMABLES</th>
<th>MATERIALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preserve capital and minimize overhead&lt;br&gt;Outsourcing is a strong trend (fabless)&lt;br&gt;Generally start at small wafer sizes and work up to 200mm</td>
<td>Not locked in to &quot;traditional&quot; CMP pad/slurry offerings&lt;br&gt;Lots of small-volume niche opportunities</td>
<td>Willing to explore a wide range of materials for unique properties&lt;br&gt;Process requirements vary by several orders of magnitude</td>
</tr>
</tbody>
</table>

### Summary

- Many products not even based on traditional CMOS
- Startup or new entry mentality
- Frequently start on smaller wafer sizes and transition up as production volume increases
- Integration and/or process technology are generally not mature due to some fraction of “creative” steps
- Design focus = new devices
- Process focus = acceptable yields

### Outlook

- Materials and process challenges can be very unique.
- Volumes tend to start low, but some devices ramp fast.
- Not as cost sensitive during development (later)
- Defect levels vary wildly depending on the product.
- Generally more willing to try new consumables.
- Companies include a wide range from new startups to other industries to specialized development teams within major semiconductor manufacturers.
CMP is continues to evolve for CMOS... But new applications are also being developed well beyond “traditional” CMP.

- **MEMS**
  - Oxides (doped or undoped)
  - Polysilicon (often structural)
  - Nitrides and oxynitrides
  - Separation layer (MEMS-first or MEMS-last)
  - Metals (Au, Pt, Al)

- **Advanced Substrates**
  - Strained layer epi substrates
  - Custom III-IV and II-IV epi layers
  - SOI
  - AlN, diamond, GaN, InGaP, SiC, GaAs, etc.
  - Various surfaces for direct wafer bonding

- **Integrated Optics**
  - Grating structures
  - Embedded waveguides
  - Integrated optical elements

- **Other**
  - Phase change memory materials
  - Photoresist and other polymers
  - Refractory metals
  - Magnetic materials (active or shielding)
  - Advanced packaging (TSV)
  - 3D IC’s and similar device technologies
### CMP Applications

<table>
<thead>
<tr>
<th>1995 - Qty ≤ 2</th>
<th>2001 - Qty ≤ 5</th>
<th>CMOS</th>
<th>2011 - Qty ≥ 40</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMOS</strong></td>
<td><strong>CMOS</strong></td>
<td><strong>CMOS</strong></td>
<td><strong>New Apps</strong></td>
</tr>
<tr>
<td>Oxide</td>
<td>Oxide</td>
<td>Oxide</td>
<td>MEMS</td>
</tr>
<tr>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Nanodevices</td>
</tr>
<tr>
<td>Cu (Ta barrier)</td>
<td>Cu (Ta barrier)</td>
<td></td>
<td>Direct Wafer Bond</td>
</tr>
<tr>
<td>Shallow Trench</td>
<td>Shallow Trench</td>
<td></td>
<td>Noble Metals</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td></td>
<td>Through Si Vias</td>
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<tr>
<td>Low k</td>
<td>Low k</td>
<td></td>
<td>3D Packaging</td>
</tr>
<tr>
<td>Capped Ultra Low k</td>
<td>Ultra Thin Wafers</td>
<td></td>
<td>Diamond &amp; DLC</td>
</tr>
<tr>
<td>Metal Gates</td>
<td>NiFe &amp; NiFeCo</td>
<td></td>
<td>Si and SOI</td>
</tr>
<tr>
<td>Gate Insulators</td>
<td>Al &amp; Stainless</td>
<td></td>
<td>Lithium Niobate</td>
</tr>
<tr>
<td>High k Dielectrics</td>
<td>Detector Arrays</td>
<td></td>
<td>Quartz &amp; Glass</td>
</tr>
<tr>
<td>Ir &amp; Pt Electrodes</td>
<td>Polymers</td>
<td></td>
<td>Titanium</td>
</tr>
<tr>
<td>Novel barrier metals</td>
<td>Magnetics</td>
<td></td>
<td>Sapphire</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Integrated Optics</td>
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</tbody>
</table>

- **Substrate/Epi**
  - GaAs & AlGaAs
  - poly-AlN & GaN
  - InP & InGaP
  - CdTe & HgCdTe
  - Ge & SiGe
  - SiC
  - Diamond & DLC
  - Si and SOI
  - Lithium Niobate
  - Quartz & Glass
  - Titanium
  - Sapphire
  - Integrated Optics
Our Expertise, Our Services, Your Success

Comprehensive CMP Solution

#1 Accelerate Time to Revenue
#2 Reduce Cost and Risk
Value Proposition

CMP Foundry

- Rapid Technology Advancement
- Cost Reduction
- Integration of New Materials
- Consumable Screening
- Process Development
- Yield Enhancement

Remanufactured Polishers

- IPEC (Novellus): 372M; 472; 676; 776
- SpeedFam (Novellus): CMP-V; Auriga; Auriga-C; Auriga-EC
- Ebara: EPO-220; EPO-222; F-REX 200; F-REX 300
- AMAT: Mirra 3400, Mirra Trak, Desica, Mirra Mesa, Reflexion
- Strasbaugh: 6DS-SP(nTegrity); 6EG(nHance); 6EC(nSpire)
Thank you

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