



# Advanced Lithography and Inspection Solutions for 3D TSV Packaging of MEMS Devices



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# Outline



- Introduction EV Group
- Why 3D TSV Packaging of MEMS?
- Characteristic Requirements of 3D Packaged MEMS Devices
- Lithography and Inspection Solutions for 3D TSV Packaging of MEMS
- Summary and Conclusion



# EV Group at a Glance



EV Group (EVG) is a global supplier of

- **Wafer Bonders**
- **Aligners**
- **Coaters / Developers**
- **Temporary Bonders / Debonders (Laminator)**
- **Cleaners**
- **Inspection Systems**

EV Group (EVG) is a global supplier to

- **Advanced Packaging, 3D Interconnect**
- **MEMS (MicroElectroMechanical Systems)**
- **SOI (Silicon-On-Insulator)**
- **Compound Semiconductor and Silicon based Power Devices**
- **Nanotechnology**

EV Group holds the dominant share of the market for wafer bonding equipment (especially SOI bonding) and is a leader in lithography for advanced packaging and nanotechnology.

# EV Group at a Glance



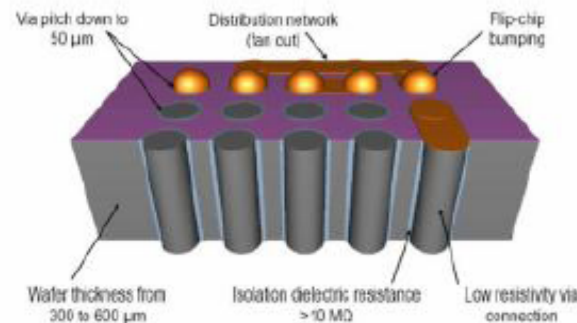
- Founded in 1980
- Installed base in excess of 1,500 tools world wide in High Volume Production and R&D
- Corporate headquarters in Austria – subsidiaries in JP, KR, TW and US
- Approx. 480 employees worldwide
- World wide sales and customer support organization
- R&D investment: 20 % of sales revenue



# Why 3D TSV Packaging of MEMS?

## 3D MEMS

- Today we are moving from **Wafer Level Capping** to **Wafer Level Packaging**, with **through Si Via** interconnects
- **3D TSV**
  - Today this is an industrial reality with continuous growth expected.
  - Companies like Dalsa, Silex, IMT, ePack proposes 3D TSV.
  - The need for smaller, more performing MEMS for consumer applications will favor this technology.
  - Cost is the major issue
    - Wire bonding remains the cheapest assembly technology. It will still be used for low margin products with no performance/form factor constraints. 3D TSV brings increased form factor and performance but it is still an expensive technology
  - The 2009 crisis might delay the introduction of this technology but we believe 3D TSV will be increasingly used.



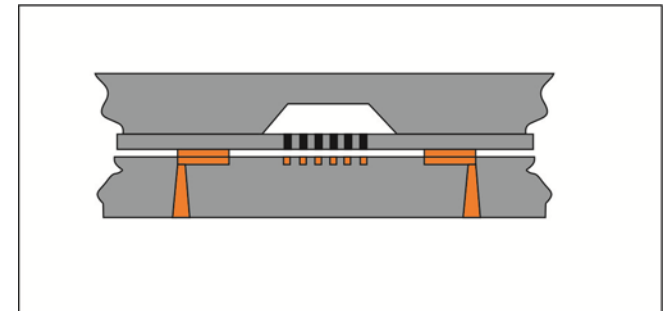
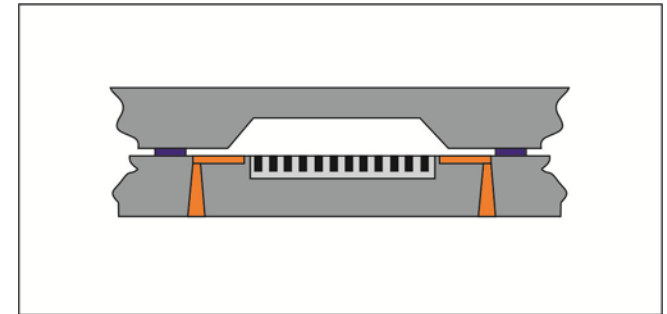
TSV platform from Silex

# Why 3D TSV Packaging of MEMS?



There are two application scenarios for 3D TSV Packaging of MEMS

- As a means for more advanced packaging, offering form factor (size) and performance advantages.
- To enable integration of two functional wafers



# Characteristic Requirements of 3D Packaged MEMS Devices



# Advanced Lithography Solutions



- Precise Alignment
  - Front-side Alignment
  - Front-to-Backside Alignment
- Automation
- CD Uniformity
- IR Alignment (TIR and RIR)
- Ability to handle thin wafers
- Ability to expose on wafers with topography



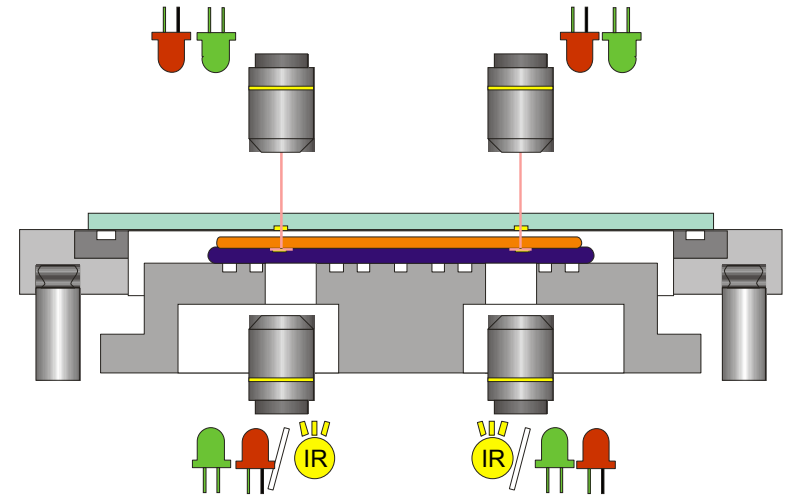
# Alignment Modes

The EVG IQ Aligner can be configured with:



- **Topside Microscopes enabling**
  - Topside **live** alignment
  - Large gap alignment  
(Typically for thick resist applications  $\sim > 30\text{-}50\mu\text{m}$ )
  - Dark field mask alignment
  - Flat alignment
  - **IR** alignment (no mechanical adjustments just recipe selected)
  - Precision insitu alignment (in-liquid)

- **Bottomside Microscopes enabling**
  - Backside alignment
  - Backside large gap alignment  
(Typically carrier mounted substrates)
  - Bond alignment (optional with IR)
  - IR alignment (for Bond Alignment)



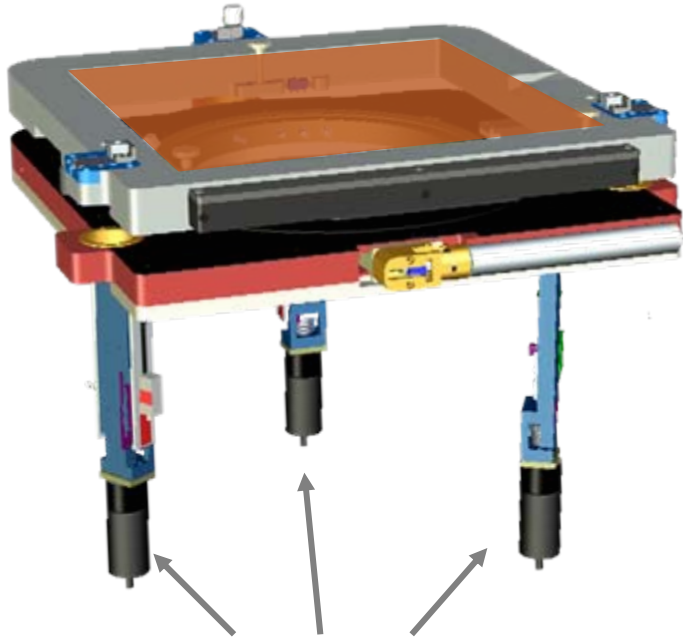
# Stage Design



## ■ 3 Motorized Z-Spindles

### ■ Technical benefit:

- Lithography - 100% contactless proximity processing  
(in combination with external wafer thickness measurement)



Motorized Z-Spindles  
for accurate alignment-  
and exposure gap setting



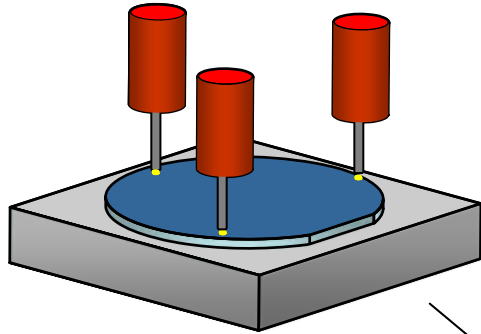
# External Wafer Thickness Measurement



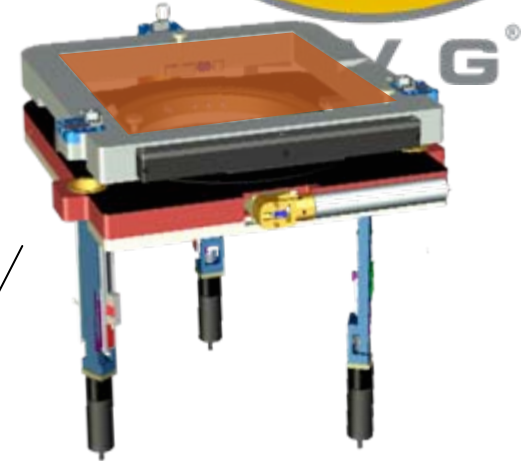
- Wafer thickness measurement at 3 positions integrated on automatic handling module
- Min. contact force (field proven)
- Highest repeatability compared to optical measurements (wafer surface property variations!)
- Average measurement spot ~1mm equalizing topography
- No contact between wafer and mask at any time (for proximity exposures process)



# 100% Contactless Proximity Processing

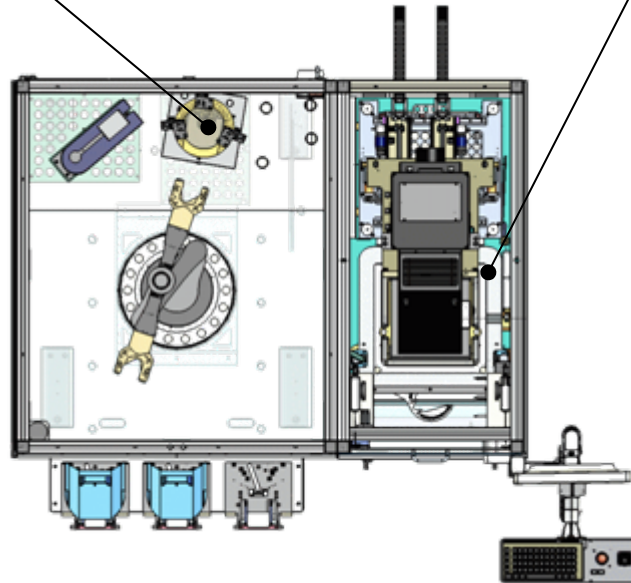


Wafer thickness/wedge data



## Wafer Thickness Measurement

Wafer wedge information eliminates the internal wedge error compensation sequence with wafer against mask inside the aligner module.



## Alignment Stage

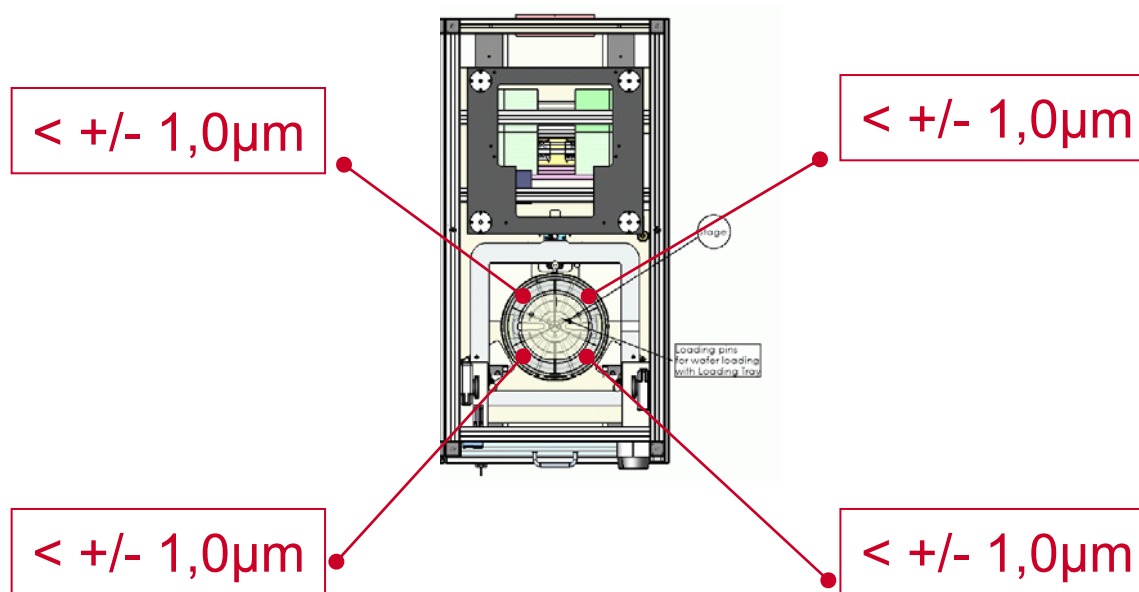
Wafer thickness data is directly transmitted to aligner stage. Accurate Z-position (alignment gap, exposure gap) for each spindle drive can be calculated hence avoiding the use of proximity spacer tooling and any contact between wafer and mask.

Therefore 100% contact free processing possible!

# EVG IQ Aligner<sup>®</sup> – Print Gap Repeatability

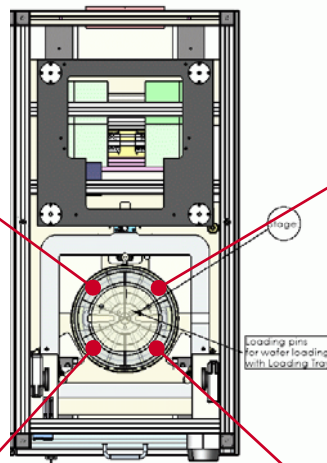
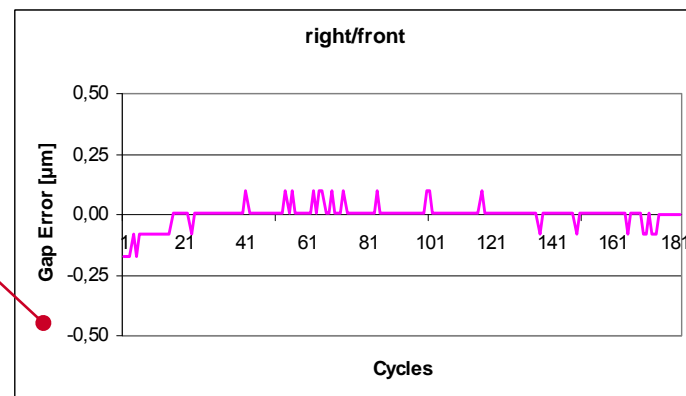
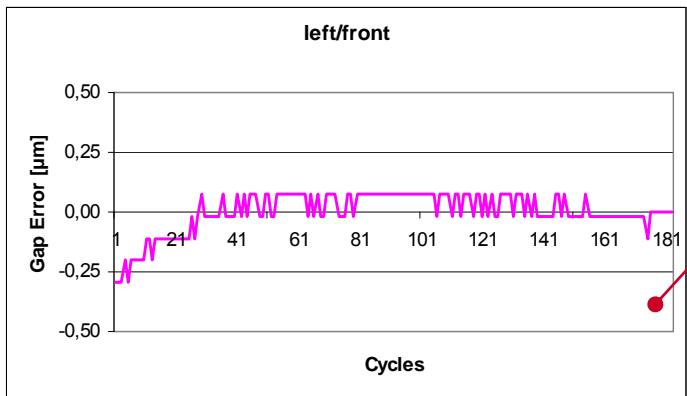
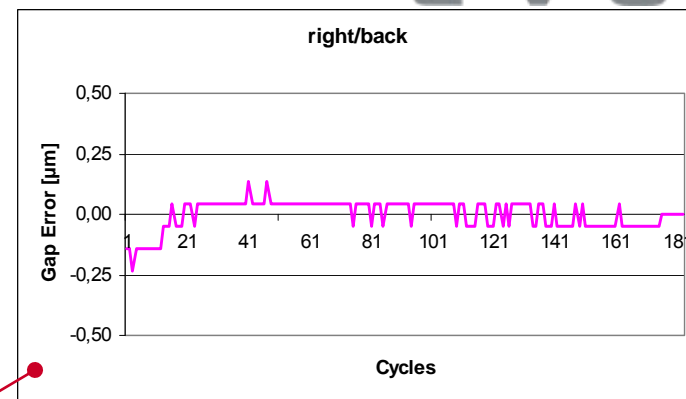
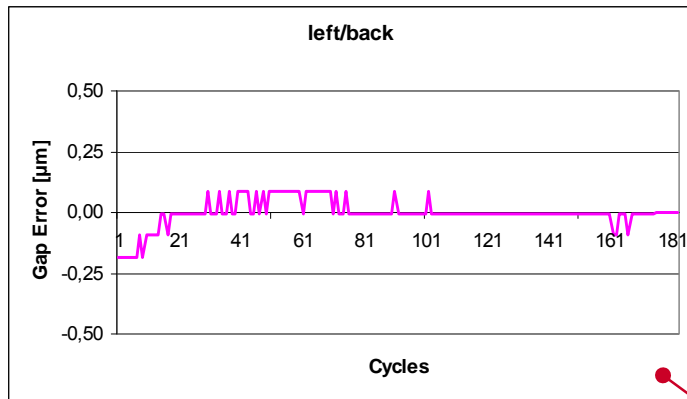


- Homing Repeatability Data < +/- 0,5 $\mu$ m
  - Positioning Repeatability Data < +/- 0,5 $\mu$ m
- 
- Print Gap Repeatability < +/- 1,0 $\mu$ m



\* Measured on 200mm diameter

# EVG IQ Aligner<sup>®</sup> – Positioning Repeatability Data



\* Measured on 200mm diameter

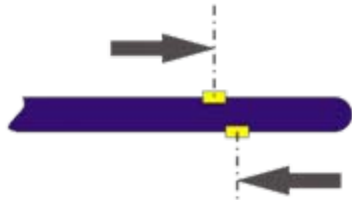
# Advanced Inspection Solutions



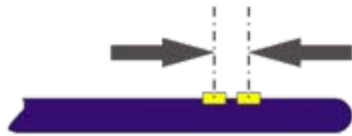
- Inspection for Lithography
  - Front-side Overlay
  - Front-to-Backside Overlay
  - Alignment to buried alignment keys
  - CD Uniformity
  - Data Feed Forward to Aligner
- Inspection for Bond Alignment
  - Data Feed Forward to Aligner



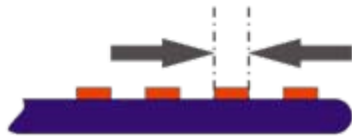
# EVG<sup>®</sup>40NT Operation Modes: Lithography



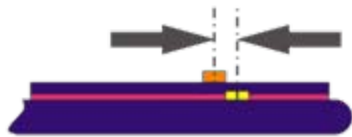
- **Front-to-Back Alignment (BSA)**  
Accuracy:  $<0.1\mu\text{m}$  (3 Sigma);



- **Top Side Alignment (TSA), Overlay or Box-in-Box**  
Accuracy:  $<0.1\mu\text{m}$  (3sigma)



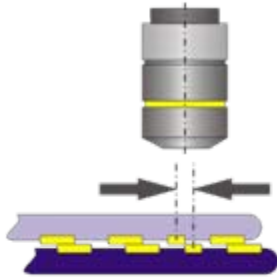
- **Critical Dimension (CD)**  
Accuracy:  $<0.1\mu\text{m}$  (3sigma)



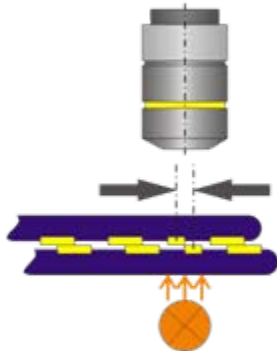
- **Alignment to Bond Interface (Via IR Inspection)**  
Accuracy:  $<0.1\mu\text{m}$  (3sigma)



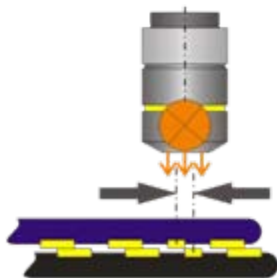
# EVG<sup>®</sup>40NT Operation Modes: Bonding



- **Bond Alignment with Visible Light**  
Accuracy:  $<0.1\mu\text{m}$ (3sigma)



- **Bond Alignment with Transmitted IR**  
Accuracy:  $<0.1\mu\text{m}$  (3sigma)

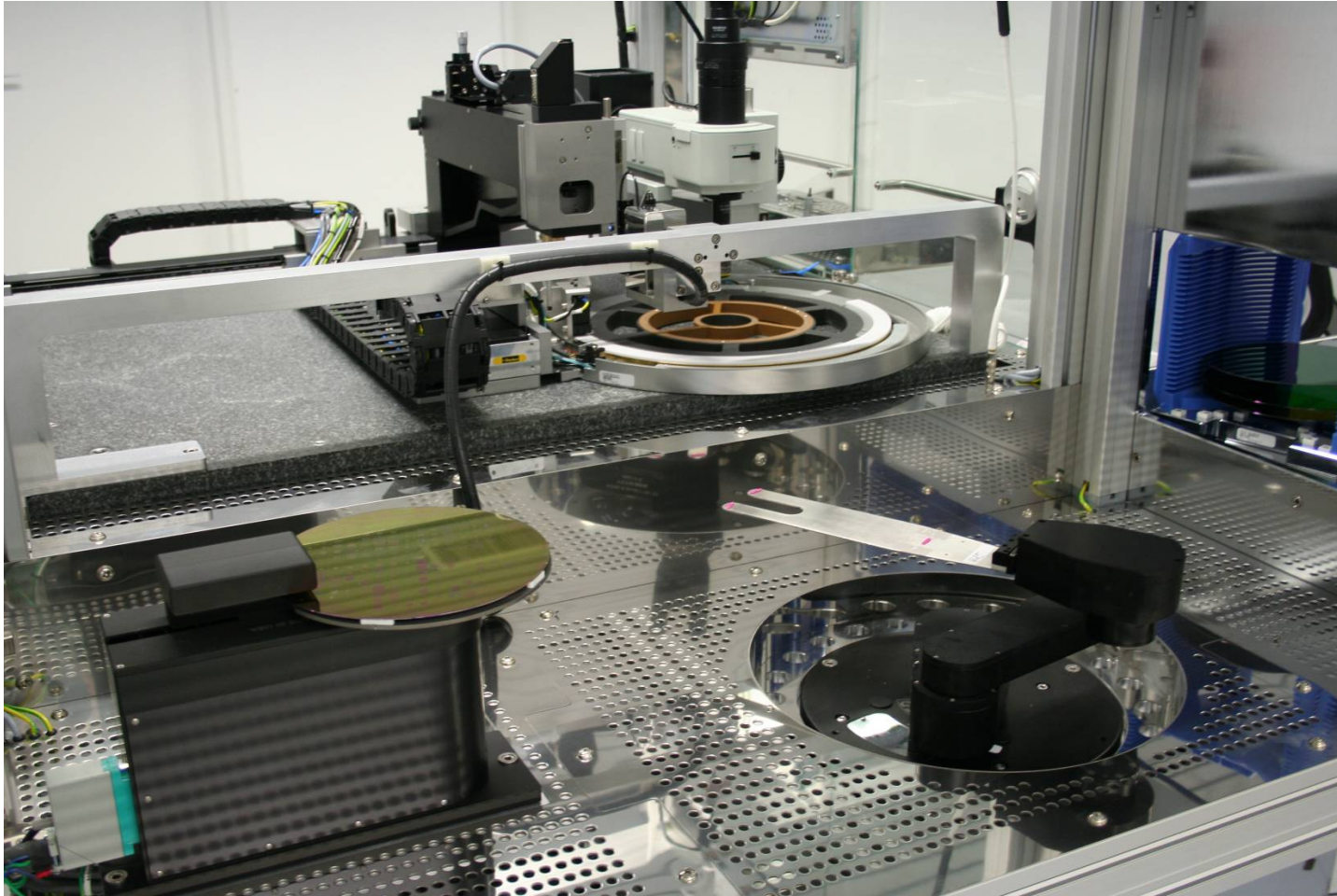


- **Bond Alignment with Reflected IR**  
Accuracy:  $<0.1\mu\text{m}$  (3sigma)



# EVG<sup>®</sup>40NT: System Design

(Fully Automated)



**SEMICON<sup>®</sup>**  
*Taiwan2011*

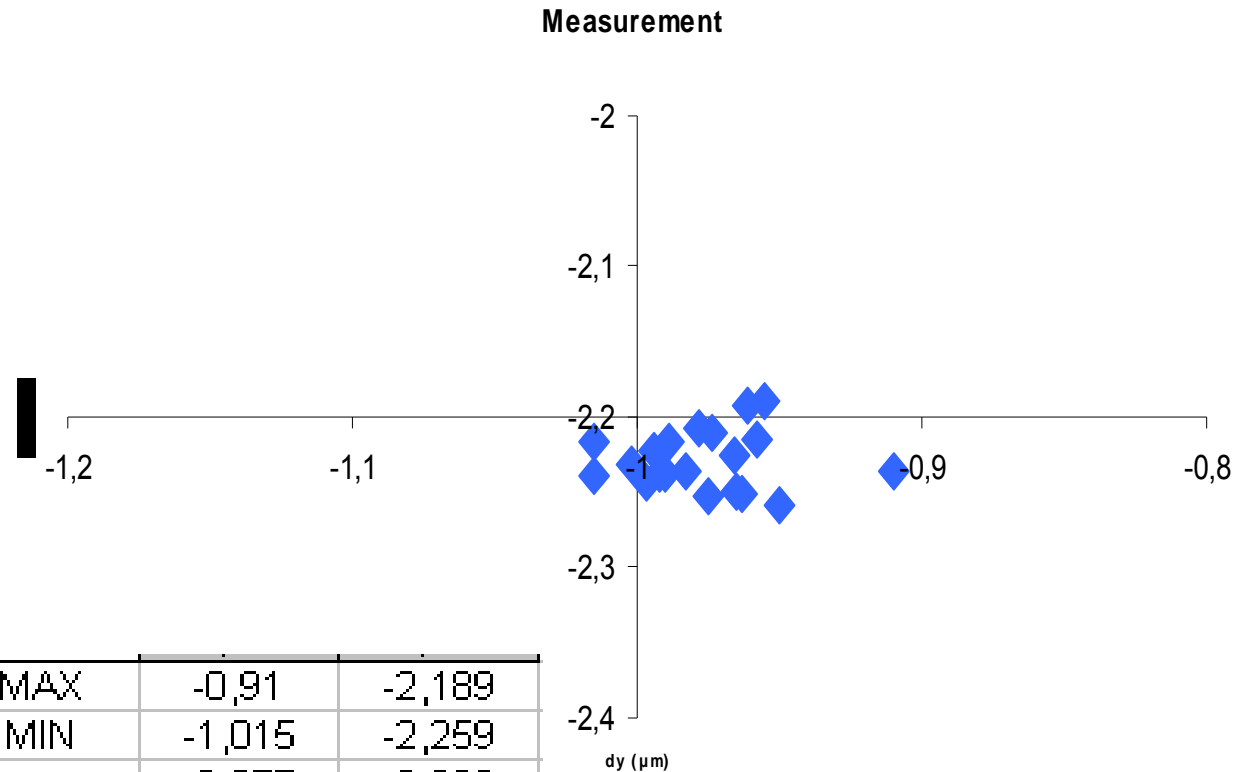
\*Windows is a registered trademark of Microsoft Corporation

# EVG<sup>®</sup>40 NT: Measurement Results



## Transmitted Infrared:

Reproducibility IR		
Run	Result	
	X	Y
1	-0,965	-2,249
2	-0,983	-2,236
3	-0,99	-2,238
4	-0,95	-2,259
5	-0,975	-2,253
6	-0,958	-2,215
7	-0,974	-2,21
8	-0,966	-2,226
9	-0,91	-2,236
10	-0,989	-2,216
11	-0,963	-2,251
12	-0,961	-2,192
13	-1,015	-2,239
14	-0,994	-2,222
15	-0,978	-2,208
16	-1,002	-2,231
17	-1,015	-2,216
18	-0,997	-2,244
19	-0,992	-2,238
20	-0,955	-2,189
MAX	-0,91	-2,189
MIN	-1,015	-2,259
Average	-0,977	-2,228
Sigma	0,025	0,020
<b>3*Sigma</b>	<b>0,074</b>	<b>0,059</b>

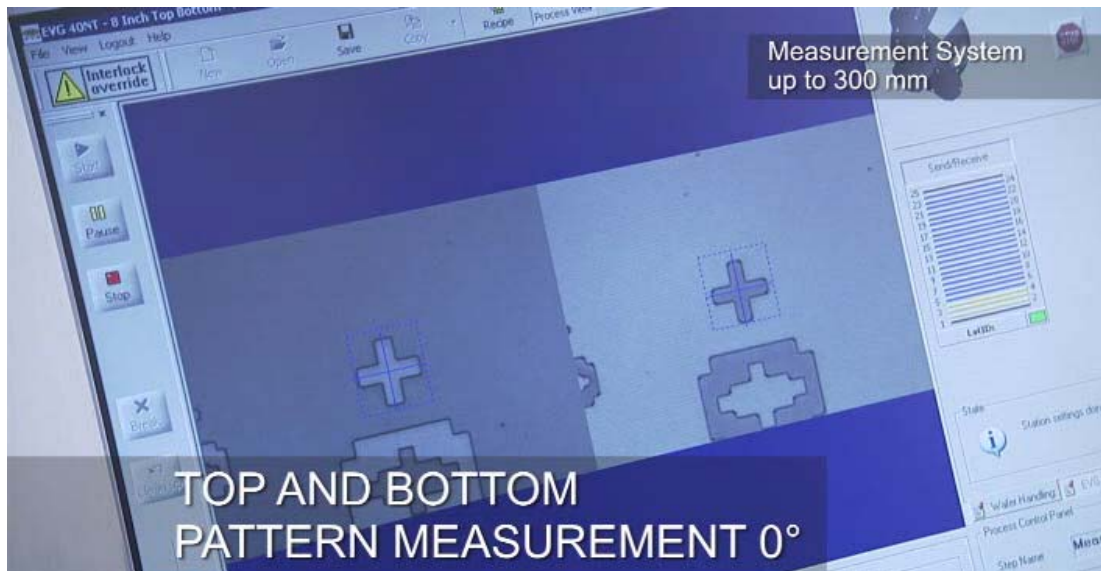
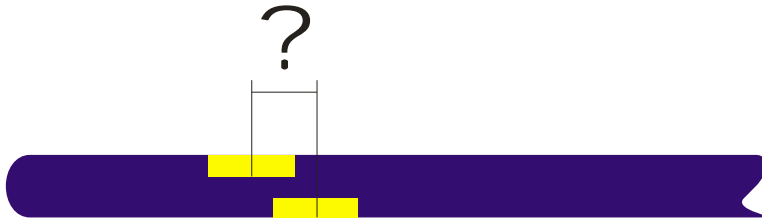


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<b>3*Sigma</b>	<b>0,074</b>	<b>0,059</b>

# EVG<sup>®</sup>40NT: Working Principle T/B



- Alignment keys as used for double sided lithography are selected



# EVG<sup>®</sup>40NT: Working Principle T/B



- Image of top and bottom side microscope is shown on split field monitor

Microscope

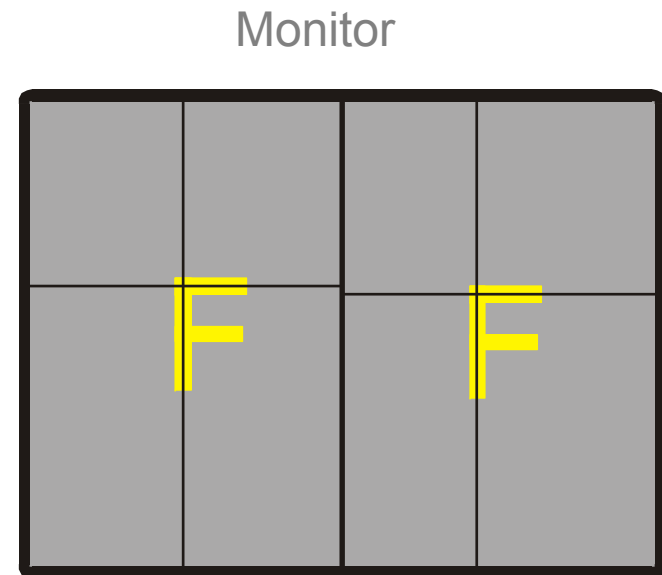
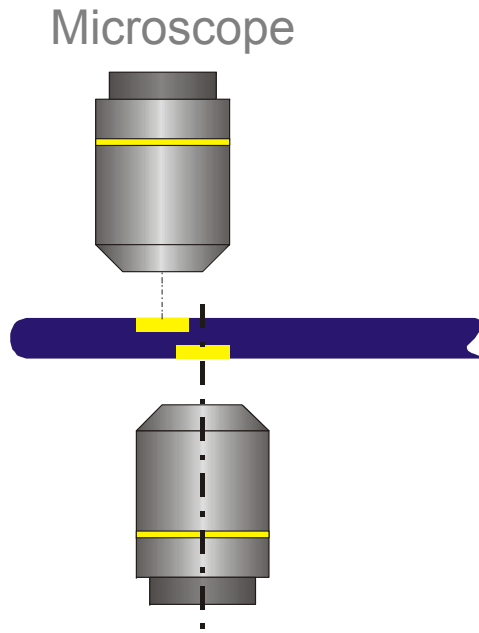
Monitor



# EVG®40NT: Working Principle T/B



- Alignment keys are adjusted into field of view
- Alignment key positions of top and bottom pattern are digitized

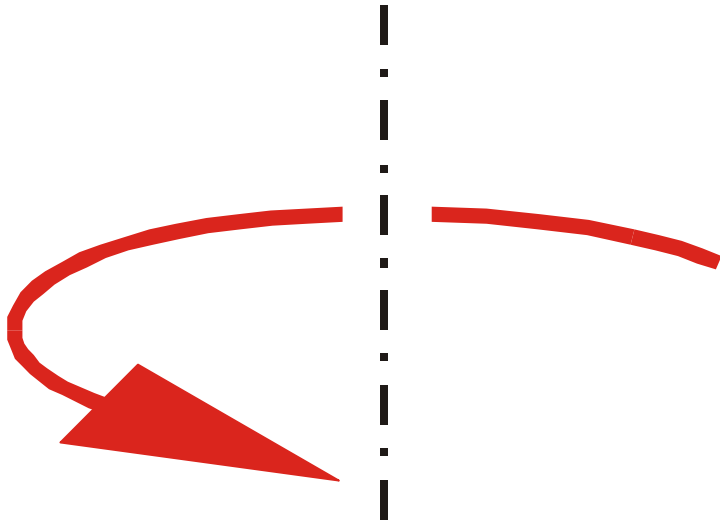


# EVG®40NT: Working Principle T/B

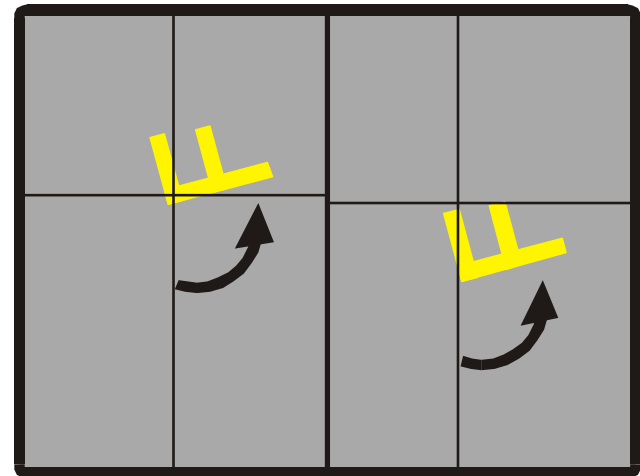


- Wafer is rotated by 180°

Microscope



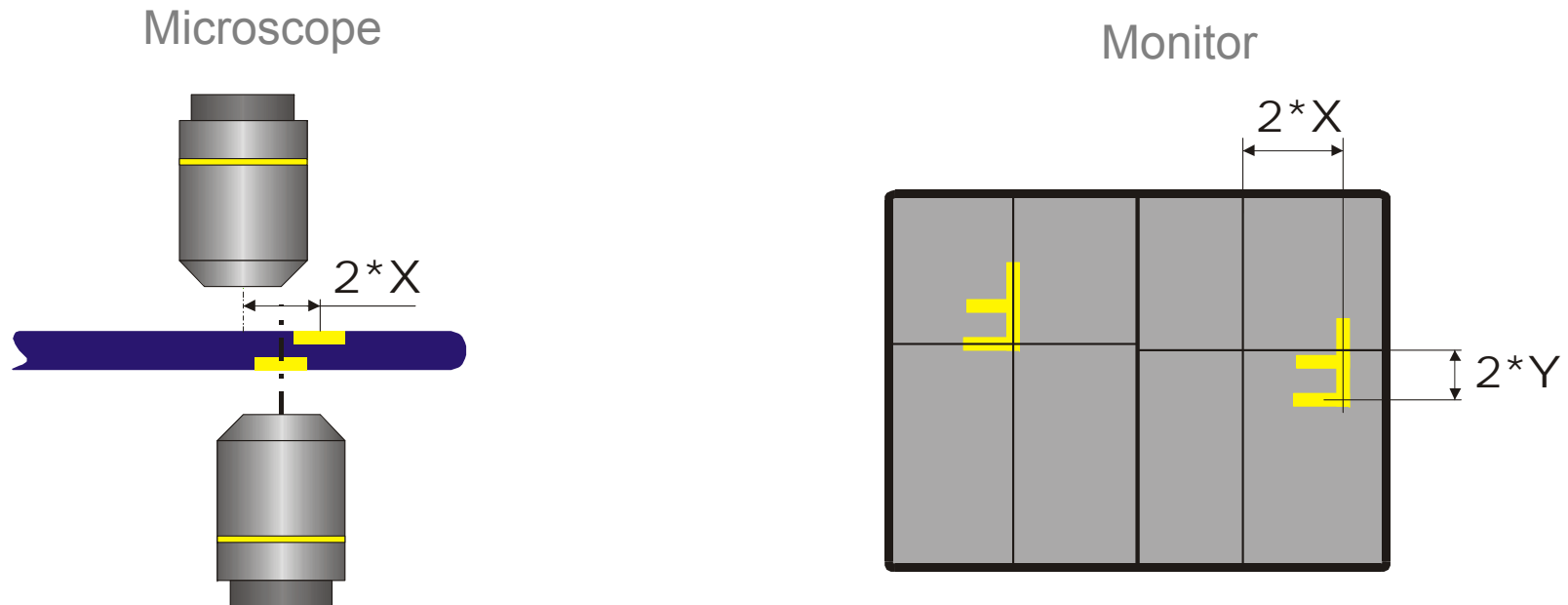
Monitor



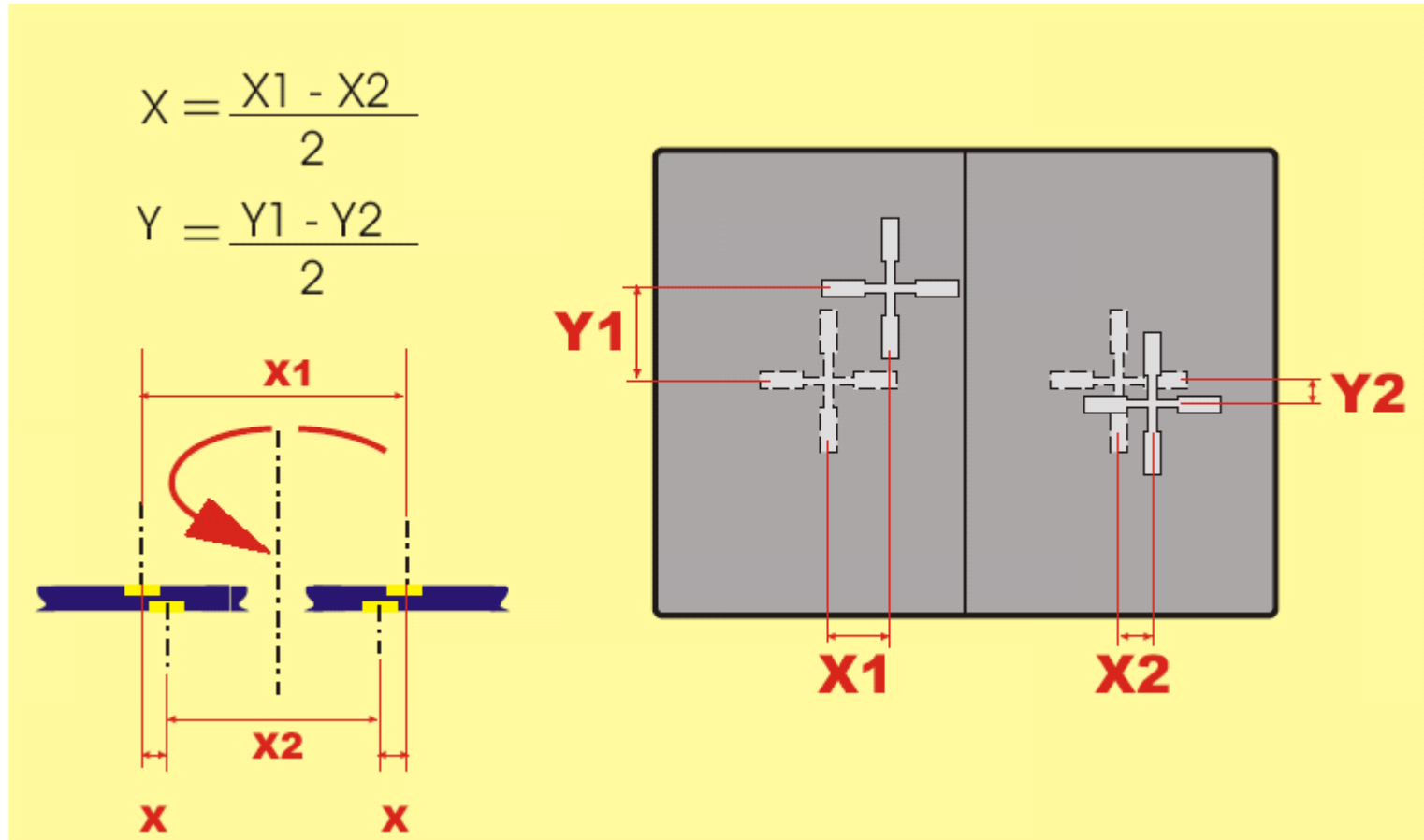
# EVG®40NT: Working Principle T/B



- Alignment key position is digitized again and alignment accuracy is calculated
- Misalignment is shown as doubled offset compared to the originally stored position

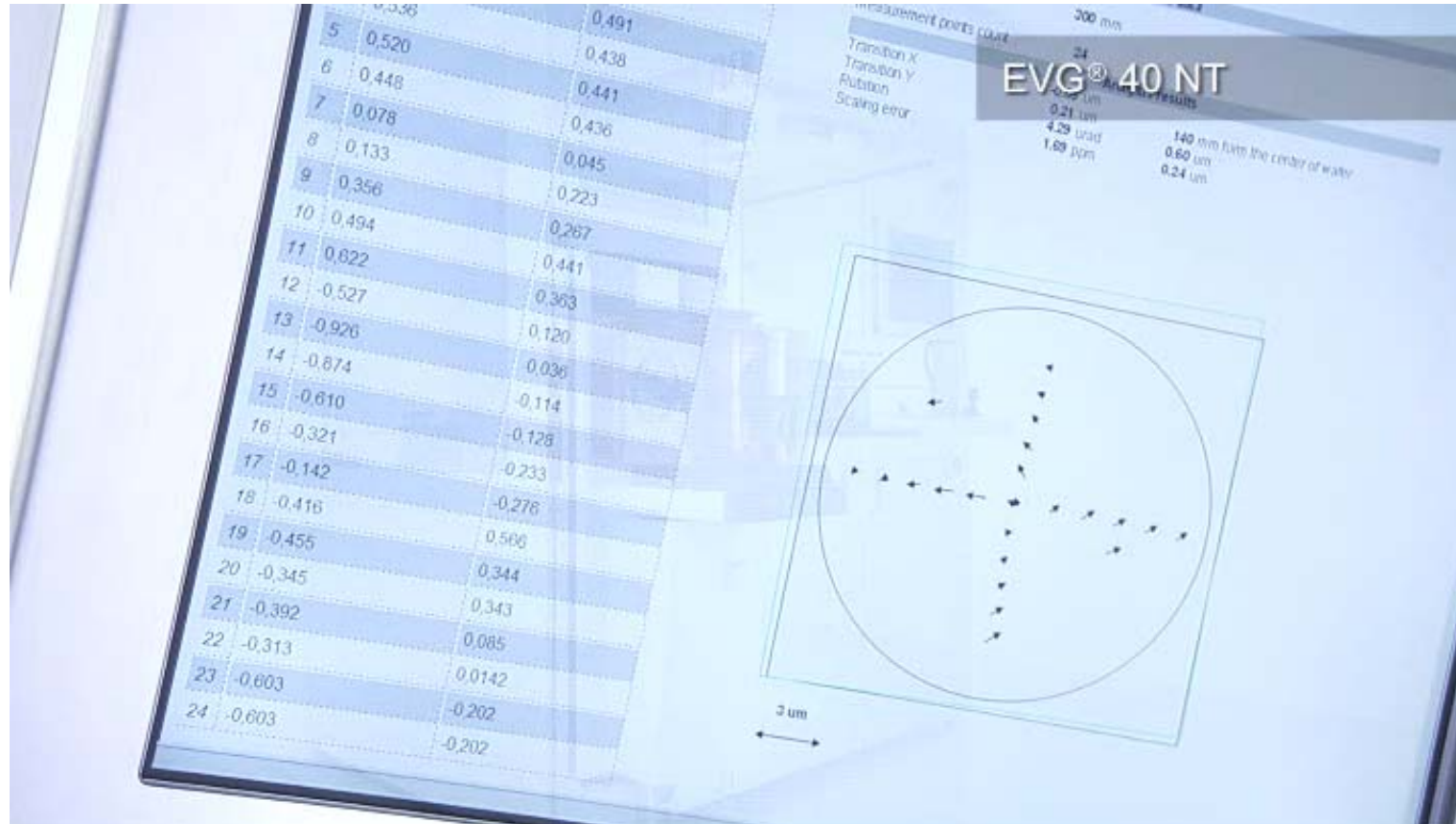


# EVG<sup>®</sup>40NT: Calculation of Misalignment for T/B



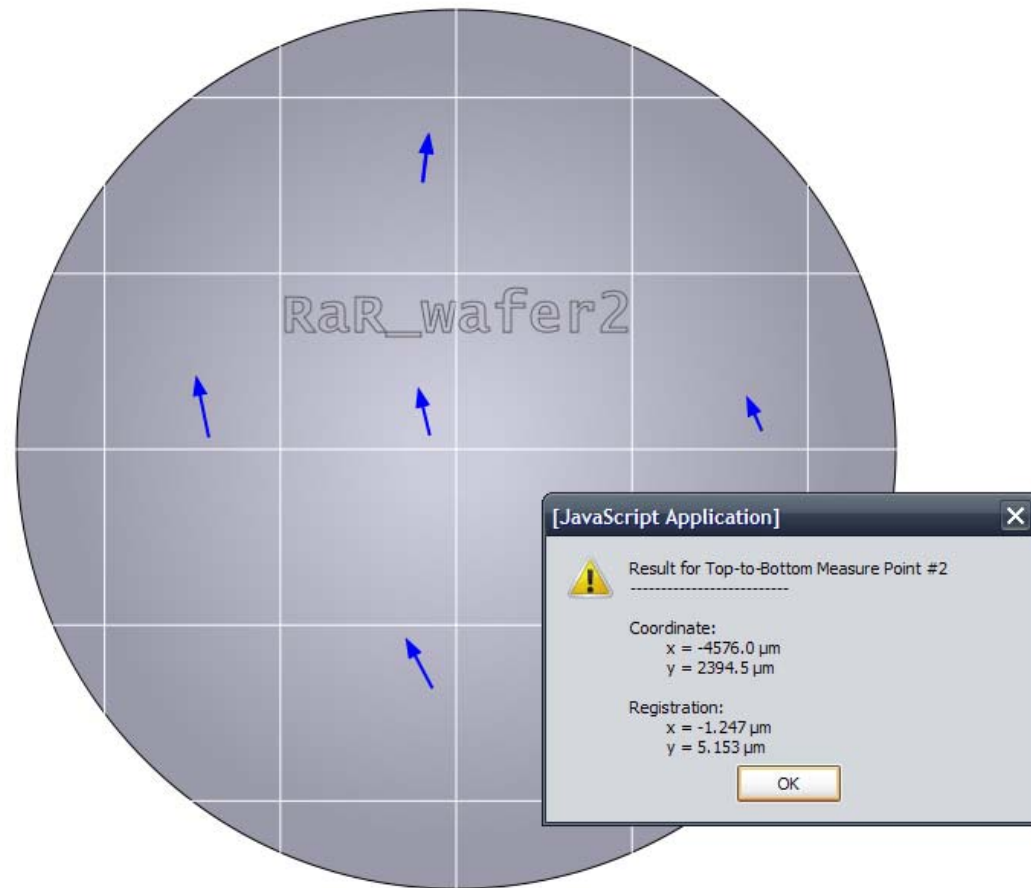
# Output of Measurement

Wafer map of measured points



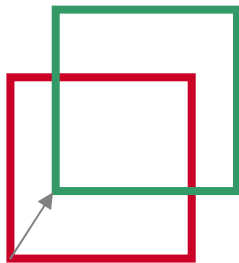
# Detailed view of wafer

- All points are displayed
- Each point can be displayed in detail

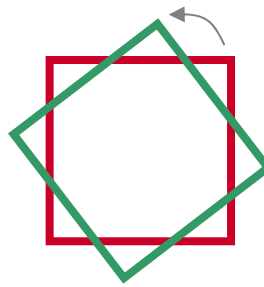


# Overlay theory

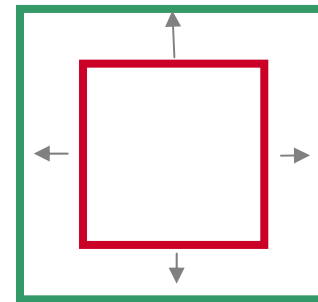
- The P2 and P1 after alignment could show following misalignment errors (assuming simplest linear model):
  - Transition in X-direction [ $\mu\text{m}$ ]:  $T_x$
  - Transition in Y-direction [ $\mu\text{m}$ ]:  $T_y$
  - Mask rotation [ $\mu\text{rad}$ ]:  $R$
  - Mask run-out error (magnification/scale for steppers) [ppm]:  $M$
  - The rest is error of the model (distortion):  $e_x, e_y$



Transition



Rotation



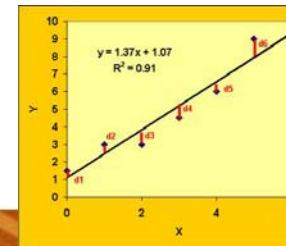
Mask run-out error

# Overlay model equations

- Each registration has to fulfill following equations:

$$\begin{aligned} \Delta_x &= T_x + M * x + R * y + e_x \\ \Delta_y &= T_y + M * y + R * x + e_y \end{aligned}$$

- Where  $\Delta_x$ ,  $\Delta_y$  is measured misalignment on x,y position on wafer (calculated from center of the wafer)
- This could be done by multiple linear regression (least squares) (excel function LINEST())

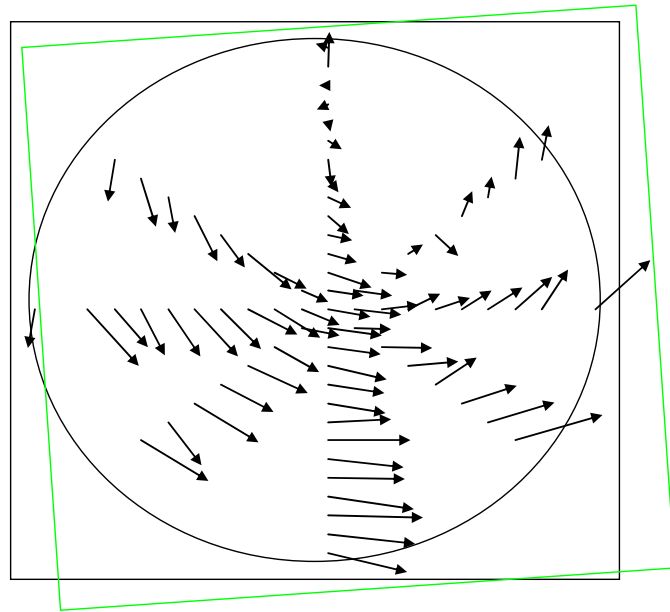


# Modeled



- Measured

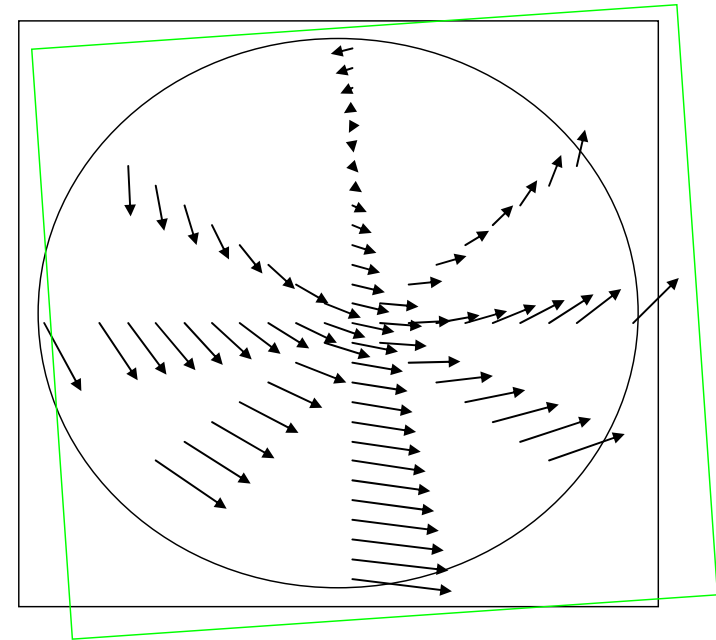
Analysis results		
Transition X	1.47 um	
Transition Y	-0.46 um	140 mm form the center of wafer
Rotation	15.77 urad	2.21 um
Mask-run out	0.96 ppm	0.13 um
Residual error (rms)	12.86 um <sup>2</sup>	
Goodness of fit	85%	Model fits the data



3.85 um

- Modeled

Analysis results		
Transition X	1.47 um	
Transition Y	-0.46 um	140 mm form the center of wafer
Rotation	15.77 urad	2.21 um
Mask-run out	0.96 ppm	0.13 um
Residual error (rms)	0.00 um <sup>2</sup>	
Goodness of fit	100%	Model fits the data



3.76124094517861 um



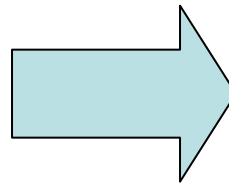
# Interaction with EVG Aligner

## Data transfer to EVG Aligner

- Data correction for:
  - Transition x
  - Transition y
  - Rotation
  - Run out
- Transfer via Secs/Gem

$$\Delta_x = T_x + M * x - R * y + e_x$$

$$\Delta_y = T_y + M * y + R * x + e_y$$



# Summary & Conclusions



- Advanced MEMS products require advanced manufacturing solutions
- With MEMS devices getting smaller, tolerances are getting tighter, driving the need for more accurate alignment and sophisticated inspection solutions.
- Leading edge solutions for optimized results on Mask Aligners have been presented.
- Sophisticated metrology solutions for the manufacture of advanced MEMS devices, including data feed forward functionality have been presented.



Thank you for your attention!

Please visit our booth #2506

