Different Drivers – Continuous Growth

Source: IHS Q2 2015

Mobile Computing
- 1981, IBM PC MS-DOS
- 1986
- 1991
- 1996
- 2001
- 2006
- 2011
- 2016

Sensing
- 2001 - 3G Cellphones
- 2002 - Cellphones w/ camera
- 2007 - iPhone
- 2010 - iPad

Enhancement

B USD

Technology Roadmap: Continuous Innovation

- Functional Diversification
  - Wire-Bonding
  - Homogeneous
  - Heterogeneous
- More than Moore
  - Advanced Packaging (3DI / WLP)
  - Si Photonics
  - Emerging Memory
- More Moore
  - Patterning
  - New Material
  - New Structure

Technology Roadmap: Continuous Innovation

- CMOS Scaling
  - Krf
  - ArF
  - ArF-Immersion
  - EUV
- More than Moore
  - DP/MP
  - NIL, EBDW
- Emerging Memory
  - STT-MRAM
  - ReRAM
  - 3D NAND
- New Material
  - High-k Metal Gate
  - Cu/ELK
- Patterning
  - FinFET
  - Cu/ULK

Source: Tokyo Electron Limited (based on ITRS)
Patterning Destination Set by Device Technology

**DRAM**

- SEM Image: TEL AR > 50

**3D NAND**

- Planar STI
- 193 Dry Exposure
- FinFET STI
- SADP + Cut (x1 – 2)
- Nanowire STI
- SAQP + Cut (x2 – 3)

**Logic**

- 22nm (FinFET RMG)
- C. Auth, et al., VLSI Tech. 2012
- T. Ghani, et al., IEDM 2003
- R. Coquand et al., VLSI Tech. 2013
Patterning Paths Which to Choose?

**EUV**
- Process Simplicity
- Design Flexibility

**Multiple Patterning**
- Pitch Scalability
- Production Ready

**DSA**
- Low CapEx
- Materials Enabled Shrink

Promise
- Process Simplicity
- Pitch Scalability
- Low CapEx
- Design Flexibility
- Production Ready
- Materials Enabled Shrink

Challenge
- High CapEx
- Edge Placement Error (EPE)
- Self Alignment Defect
- Tool Productivity
- Process Complexity
- Design Flexibility

Source: IMEC 2015
Patterning at a Crossroads
Immersion Multiple Patterning
Patterning Superhighway
Immersion Multiple Patterning Process

Pre Pattern
193i Single Patterning
- Litho
- Material Process
- LER Reduction
- CDU Control

Grid Formation
SAMP (DP, QP, OP)
- Deposition
- Etch
- LER Reduction
- CDU Control
- Spacer Selectivity

Cut Pattern
LE\textsuperscript{x} Multiple Patterning
- Litho (193i, EUV)
- Planarization
- Etch
- Hole Shrink
- Pattern Healing
- Variation Control

Pattern Memorization
Line Cut
- Etch
- Deposition
- Self Alignment
- Pattern Reversal
- HM Selectivity
Grid Pattern Formation
DCS & Metal Oxide Spacer

SADP Performance Enhancements

SiO₂
Photo Resist
SiARC

TiO Spacer
(Improved Selectivity)

DCS cured
(Enhanced Smoothing)

Direct Current Superposition (DCS) Technology

Ar⁺
EB
H⁺

PR Curing

Si Coating
**Grid Pattern Formation**

**DCS & Metal Oxide Spacer**

44nm hp

**Photo Resist**

- **Spacer Depo**
- **Spacer RIE**
- **Middle Layer RIE**
- **Bottom Layer RIE**

22nm hp

- **Ox spacer**
- **TiO spacer**

Improved LER & Resist Profile

- **No recess on Middle Layer**
- **Higher RIE Selectivity**
- **Improved Image Transfer**

Low temperature TiO and DCS process enable improved SADP process
Cut Pattern Formation
Healing & Shrinking

For Fin, Gate

Trench shrink for cutmask

Hole shrink
Hole multiplication

For Via, Contact

193i
Cut Pattern Formation
Healing & Shrinking

In-situ polymer deposition thru-etching

Min 63nm pitch in immersion

SiARC etch  SOC etch  Oxide etch  Ashing

PR  SiARC  SOC  TEOS

63nm 63nm 63nm 63nm

14nmΦ

Cut Pattern Formation
Healing & Shrinking

In-situ polymer deposition thru-etching

Min 63nm pitch in immersion

SiARC etch  SOC etch  Oxide etch  Ashing

PR  SiARC  SOC  TEOS

63nm 63nm 63nm 63nm

14nmΦ
**Cut Pattern Formation**

*Healing & Shrinking*

**Process Window**

- ADI (49.3nm±10%)
- AEI (31.2nm±10%)

**Hole CD Healing**

- CDU 15.5nm (3sig)
- CER 3.6nm
- CER 3.4nm

**Placement Error**

- Design based

**EL**: 60% enlarged
**DOF**: 34% enlarged

**CDU**: 80% improved
**CER**: 70% improved

*TEL healing & shrinking improves overall process variability*
EUV Patterning
Waiting for the Light
Pattern Collapse Mitigation at 22nm HP

<table>
<thead>
<tr>
<th>Process Window Count</th>
<th>DIW (ref.)</th>
<th>FIRM® Extreme™</th>
<th>FIRM® Extreme™ A</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>18</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>Resolution Limit (nm)</td>
<td>22</td>
<td>20</td>
<td>19</td>
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<tr>
<td>Sensitivity at 22nm (mJ/cm²)</td>
<td>13.9</td>
<td>14.3</td>
<td>13.9</td>
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<tr>
<td>LWR at 22nm (nm)</td>
<td>6.4</td>
<td>6.2</td>
<td>5.7</td>
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</table>

Resolution and LER improvement achieved using surfactant rinse FIRM® Extreme™ A

Pattern Size
22nm Half pitch (Top-Down SEM Image)
CLEAN TRACK™ LWR & CER Improvement

TEL vapor phase smoothing process can improve LWR and CER

10.3% Improved
11.8% Improved
13.5% Improved
11.3% Improved
13.8% Improved

TEL – Jun Sung Chun / SEMATECH et. al, SPIE2014
Etch Hardening & LER Improvement

- 13.5nm EUV Resist Base

FTIR Data for cured & un-cured resist

VUV cure can modify chemical structure of EUV resist leading to smoothing

~ 20-30% improvement in roughness for optimized cure process as compared to non-cure
DSA Patterning

Order From Chaos

Self-Aligned L/S Pitch Multiplication

Self-Aligned Hole Pitch Multiplication

Simple Pitch Multiplication with CDU/LWR Self-Healing
DSA Hole Shrink Process Flow

- Hole Guide
- Affinity Control
- BCP Coat & Bake
- PMMA Wet Dev.

Negative tone resist pattern

Affinity control processes to change template surface properties

Wet development removes PMMA core
Champion Hole Defectivity – 2015
CLEAN TRACK™ LITHIUS Pro™ Z DSA

Normalized Defect Density

- Q1/13: 1.00
- Q2/13: 0.67
- Q4/13: 0.14
- Q1/14: 0.014
- Q3/14: 0.008

- Missing Hole 27%
- On Material 25%
- DSA Failure 9%
- Others 39%
- Large Material 25%
- Small Material
- Embedded
- DSA Failure
- Line Signature
- Others
DSA Etch Overall Process Optimization

Simultaneous optimization of CDU, LER, and selectivity achieved

Position

<table>
<thead>
<tr>
<th>CD-SEM</th>
<th>X-SEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square scan 300K</td>
<td>SiARC remain: 15.5nm Btm CD: 23.5nm</td>
</tr>
<tr>
<td>CD: 21.5nm LWR: 1.84nm LER: 1.79nm</td>
<td>Center</td>
</tr>
<tr>
<td>CD: 21.9nm LWR: 1.94nm LER: 2.07nm</td>
<td>Right Middle</td>
</tr>
<tr>
<td>CD: 21.6nm LWR: 2.11nm LER: 1.98nm</td>
<td>Right Edge</td>
</tr>
</tbody>
</table>

Effect of HF RF Power

**HF Source Power [W]**

0.0 1.0 2.0 3.0 4.0 5.0 6.0

**LER, LWR [nm]**

Effect of Ion Energy

**Vpp [V]**

0.0 100.0 200.0 300.0

**LER, LWR [nm]**

Selectivity

Selectivity

Selectivity
Crossroads or Converging Paths?
Summary

New drivers for increased computing power and storage continue to demand new semiconductor technologies.

Traditional scaling is at an inflection point, requiring new innovation to enable cost effective patterning solutions.

Developing these innovations requires partnership between customers, consortia, and suppliers.

TEL is ready to support all patterning technologies...
What path do you want to follow?

TEL Patterning Solutions
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