Where is the Packaging Technology Drifting? : Speed/Flexibility

Choon Lee  I  COO and CTO
Agenda

Technology trend

Amkor packaging solution

New society proposal
Vacuum tube

Transistor invention _ 1949 year

IC invention _ 1958 year

VLSI introduction _ 1970s

ENIAC (Electronic Numerical Integrator And Computer) _ 1946

TRADIAC (TRAnsistor DIgital Computer) _ 1955

IBM System 360 _ 1964

Apple II _ 1977
Computing trend

market

Mainframe Computing Era

Personal Computing Era

Mobile Computing Era

Internet of Things Era

1950 1980 2010 2020

year
New growth driver

Price War

Competing hardware specs

With IoT

H/W innovation
Electronics in Everything – The Light Bulb

- For 70+ years the common light bulb contained no electronics.
- Then in the 1970’s, CFL bulbs included a small power converter.
- Today the LED bulb contains a power supply, driver circuits, dimmers, etc.
- Soon bulbs will contain WiFi or Bluetooth radios and microcontrollers for remote operation.
X-ray Image of the L-Prize Winning LED Lamp

Philips 12E26A60
Disassembly – Main PCB, Bottom

Source: IHS
Q) What’s the packaging solution for IoT era?

Electronics in Everything

IOT

Things Transmission Gateway Big data Decision

Big data

Decision
A) The answer is Miniaturization and Integration!
Q) What’s the technology solution for new development paradigm?

Yesterday
- Time Interval
- Debugging Time
- Formalized

Today
- No Time Interval
- No Debugging Time
- Flexible

Customer/Foundries
A) The answer is wide packaging experience and process readiness!
Amkor Packaging Experience

1980 era
- PDIP
- Metal can

1990 era
- Super BGA
- PCBGA
- TABGA
- fcBGA
- fcCSP
- Plated Bump
- WLCSP
- Vision Pak
- SIP
- MLF®
- Stacked CSP
- Memory Card
- Paste Bump
- Camera Module
- PoP
- FlipStack® CSP
- Fusion Quad®
- Thru Mold Via PoP
- FC®BGA
- MEMS microphone
- Cu Pillar Bump
- fpCSP
- 2.5D Stacks, TSV
- WLO
- POSSUM™

2000 era

2010 era
Amkor One-stop and Total Solution

Design

Simulation

Development

Production

Analysis

Testing

Technology trend
Leadframe Package Innovation

- Even matured leadframe package, the innovation named routable is achieved.
Molded Substrate: RtMLF (Routeable MLF)

- **What is RtMLF?**
  - Resin filled trace available 1L substrate (MLF)
  - Low cost and small form factor driven structure
  - For server, PC, game console as well as mobile peripheral

- **Interconnection method**
  - Wire Bonding, Flip Chip

- **Development status**
  - Body size: ~10x10mm
  - I/O count: ~176
WLCSP is moving

- Mid I/O packages are converted to WLCSP due to form factor/cost

Finer pitch: More I/O, smaller chip

BLR performance: Large die solution

Thinner WLCSP

12 x 12 rtCSP = 400 I/O

44%

8 x 8 WLCSP = 400 I/O
Apple iWatch Teardown

<table>
<thead>
<tr>
<th>PKG Type</th>
<th>Body size (mm)</th>
<th>I/O Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>① WLCSP</td>
<td>4.0x4.5</td>
<td>206</td>
</tr>
<tr>
<td>② WLCSP</td>
<td>2.0x2.2</td>
<td>20</td>
</tr>
<tr>
<td>③ CABGA</td>
<td>4.0x4.3</td>
<td>49</td>
</tr>
<tr>
<td>④ FCSCSP</td>
<td>8.6x9.9</td>
<td>460</td>
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<tr>
<td>⑤ WLCSP</td>
<td>2.0x2.0</td>
<td>36</td>
</tr>
<tr>
<td>⑥ SCP</td>
<td>8.5x10.0</td>
<td>26</td>
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<tr>
<td>⑦ WLCSP</td>
<td>3.3x4.3</td>
<td>63</td>
</tr>
<tr>
<td>⑧ WLCSP</td>
<td>4.0x4.0</td>
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</tr>
<tr>
<td>⑨ WLCSP</td>
<td>3.0x3.0</td>
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</tr>
<tr>
<td>⑩ WLCSP</td>
<td>1.4x2.7</td>
<td>8</td>
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<tr>
<td>⑪ WLCSP</td>
<td>3.0x3.0</td>
<td>36</td>
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<tr>
<td>⑫ WLCSP</td>
<td>2.1x2.3</td>
<td>25</td>
</tr>
<tr>
<td>⑬ LGA</td>
<td>2.6x3.5</td>
<td>4</td>
</tr>
<tr>
<td>⑭ WLCSP</td>
<td>3.2x3.2</td>
<td>49</td>
</tr>
<tr>
<td>⑮ WLCSP</td>
<td>4.0x4.3</td>
<td>121</td>
</tr>
<tr>
<td>⑯ WLCSP</td>
<td>0.7x1.4</td>
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<tr>
<td>⑰ LGA</td>
<td>3.0x3.0</td>
<td>16</td>
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<tr>
<td>⑱ WLCSP</td>
<td>1.5x1.5</td>
<td>9</td>
</tr>
<tr>
<td>⑲ WLCSP</td>
<td>0.75x1.5</td>
<td>6</td>
</tr>
</tbody>
</table>
WLCSP Large Die Solution

- WLCSP with mold structure is to improve solder joint performance

<table>
<thead>
<tr>
<th>BD size. (mm)</th>
<th>Die thick (um)</th>
<th>Ball size (um)</th>
<th>Ball Alloy</th>
<th>TC 1st fail</th>
<th>TC Mean life</th>
<th>Drop 1st fail</th>
<th>Drop Mean life</th>
</tr>
</thead>
<tbody>
<tr>
<td>10x10</td>
<td>350</td>
<td>250</td>
<td>SACQ</td>
<td>1225</td>
<td>2849</td>
<td>179</td>
<td>1228*</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>SB05</td>
<td>836</td>
<td>1944</td>
<td>251</td>
<td>1442*</td>
</tr>
</tbody>
</table>

* Mean life is extrapolated because failure ratio is less than 50%
New Concept Technology without TSV

- Higher Performance
- Integration
- Cost benefit

**SLIM™**
Silicon-Less Integrated Module

**SWIFT™**
Silicon Wafer Integrated Fan-out Technology

- Higher Performance
- Integration
- Cost benefit
SWIFT covers Flip Chip CSP and SiP application

Molded 12inch CoW wafer processing
- Available

Fine L/S multi RDL
- 5/5um available
- 3L RDL demonstrated

Fine pitch u-bump interconnection
- CoW chip attach with mass reflow
- 40/45um available
- 30um demonstrated

Backside pattern reveal and carrier attach
- Available

Tall Cu pillar for memory interface
- 180um tall Cu demonstrated
Logic and Memory package stack

- **Body size**
  - 8~17mm

- **Mold**
  - MUF
  - Exposed die
  - Bare die
  - Strip grinding

- **BGA ball pitch**
  - 0.35mm/0.30mm

- **Interconnection**
  - Solder bump
  - Cu pillar

- **Chip attach**
  - LAB
  - TCNCP
  - MR

- **Substrate**
  - ETS
  - Coreless

- **DAF**
  - 5um thick

- **Thin die**
  - 20um thick

- **High memory I/O**
  - Fan-in PoP
  - Fine pitch TMV (~0.2mm)

- **Interposer**
### Thin PoP Roadmap

<table>
<thead>
<tr>
<th></th>
<th>Available</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory thickness (assumption)</strong></td>
<td>0.43</td>
<td>0.39</td>
<td>0.36</td>
<td>0.35</td>
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<tr>
<td><strong>Exposed die TMV</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Bottom PKG thickness</td>
<td>0.69</td>
<td>0.60</td>
<td>0.51</td>
<td>0.48</td>
</tr>
<tr>
<td>• Total stack-up thickness</td>
<td>1.12</td>
<td>0.99</td>
<td>0.87</td>
<td>0.83</td>
</tr>
<tr>
<td><strong>Bare die TMV</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Bottom PKG thickness</td>
<td>0.69</td>
<td>0.65</td>
<td>0.63</td>
<td>0.62</td>
</tr>
<tr>
<td>• Total stack-up thickness</td>
<td>1.12</td>
<td>1.04</td>
<td>0.99</td>
<td>0.97</td>
</tr>
<tr>
<td><strong>Interposer TMV</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Bottom PKG thickness</td>
<td>0.71</td>
<td>0.65</td>
<td>0.61</td>
<td>0.59</td>
</tr>
<tr>
<td>• Total stack-up thickness</td>
<td>1.20</td>
<td>1.10</td>
<td>1.04</td>
<td>1.00</td>
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</tbody>
</table>
Packaging Trend in Sensors is Going to Fusion!

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Trim Algorithm</th>
<th>Package</th>
<th>Package Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-Axis Magnetometer</td>
<td>Data Processing</td>
<td>Non-Ferromagnetic Package</td>
<td>Discrete Sensor Packages</td>
</tr>
<tr>
<td>3-Axis Accelerometer</td>
<td>Data Processing</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>3-Axis Gyro</td>
<td>Data Processing</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>Pressure Sensor</td>
<td>Data Processing</td>
<td>Cavity Package</td>
<td></td>
</tr>
<tr>
<td>Misc: IR, Humidity Optical, Microphone</td>
<td>Sensor Fusion</td>
<td>Cavity Package</td>
<td></td>
</tr>
<tr>
<td>Mag + Accel 6DOF eCompass Sensor</td>
<td>Sensor Fusion</td>
<td>Combo Sensor Package</td>
<td>Fusion Packaging</td>
</tr>
<tr>
<td>Accel + Gyro 6DOF Sensor</td>
<td>Reference Mapping &amp; Trim</td>
<td>Cavity Combo Package or Partial Cavity Package</td>
<td>• Multi-Die w/Interconnect</td>
</tr>
<tr>
<td>Mag + Accel + Gyro 9DOF Sensor</td>
<td>Kalman Filter (or similar)</td>
<td>Cavity Combo Package or Partial Cavity Package</td>
<td>• Low Stress</td>
</tr>
<tr>
<td>Mag + Accel + Gyro + Pressure 10DOF Sensor</td>
<td>Data Processing</td>
<td>Combo Sensor Package</td>
<td>• Cavity or Partial Cavity</td>
</tr>
<tr>
<td>Misc: IR, Humidity Optical, Microphone</td>
<td></td>
<td></td>
<td>• Multi-Die w/Interconnect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Very Low Stress</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Solid, Optical or Ported Lid</td>
</tr>
</tbody>
</table>
MEMS / Sensor Products

<table>
<thead>
<tr>
<th>Available</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overmold Laminate cavity</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polymer lid cavity</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Membrane U-phone</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pre-molded (Leadframe)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pre-molded (Substrate)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposed sensor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WLCSP MEMS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U phone Pressure</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9 axis Inertial Combo</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSV possum sensor</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

MEMS / Sensor Products

- Overmold Laminate cavity
- Polymer lid cavity
- Membrane U-phone
- Pre-molded (Leadframe)
- Pre-molded (Substrate)
- Exposed sensor

WLCSP MEMS

- U phone Pressure
- 9 axis Inertial Combo
- TSV possum sensor
Technology for SiP Module

- Double side mold (*Dev.)
- Embedded (Passive component)
- Double side module (Possum)
- Molded strip grinding
- Embedded active device
- Interconnection (Wire bond/FC)
- Conformal shield Sputtering (BGA/LGA)
- Lower profile: Cavity substrate (*Dev.)
- 0080004, Passive component (*Dev.)
- I/O (2nd Ball attach)

* Dev : Under development
<table>
<thead>
<tr>
<th>Item</th>
<th>Production</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die to PKG Edge</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Comp. pad to PKG edge</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Die to Die</td>
<td>75</td>
<td>65</td>
</tr>
<tr>
<td>Non common net Comp. pad</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Common net Comp.</td>
<td>60</td>
<td>50</td>
</tr>
<tr>
<td>Metal trace to Comp.</td>
<td>80</td>
<td>70</td>
</tr>
</tbody>
</table>

**Advanced SiP Design Guideline**

- **Die to PKG Edge**: 85um (Production), 75um (Development)
- **Comp. pad to PKG edge**: 85um (Production), 75um (Development)
- **Die to Die**: 75um (Production), 65um (Development)
- **Non common net Comp. pad**: 85um (Production), 75um (Development)
- **Common net Comp.**: 60um (Production), 50um (Development)
- **Metal trace to Comp.**: 80um (Production), 70um (Development)
Amkor’s Experience with Varying End Applications

- **Memory**
  - Same die stack, Pyramid stack, side by side MCM
  - DAF, FOW, Wire Bonding Interconnection

- **Connectivity, Digital, Consumer**
  - WLCSP (FC die) and Wire Bond Stack, Crystal
  - FC+ 2 die stack, die to die bonding, die to PCB bonding
  - MUF (Mold Under Filling)

- **Automotive, Sensor**
  - Sensor Die expose –Film assist molding
  - Double side assembly, Possum FC die
  - TSV, CoC stack
## SiP Technology

<table>
<thead>
<tr>
<th>Available</th>
<th>2015</th>
<th>2016</th>
</tr>
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<tbody>
<tr>
<td>IPD (Customer consigned)</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
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<tr>
<td>Core-Less Substrate Pkg</td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>Embedded Passive / Die</td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td>Possum FC</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
</tr>
<tr>
<td>Two Side assy</td>
<td><img src="image9.png" alt="Image" /></td>
<td><img src="image10.png" alt="Image" /></td>
</tr>
<tr>
<td>Compartment Shield</td>
<td><img src="image11.png" alt="Image" /></td>
<td><img src="image12.png" alt="Image" /></td>
</tr>
<tr>
<td>Conformal Shield</td>
<td><img src="image13.png" alt="Image" /></td>
<td><img src="image14.png" alt="Image" /></td>
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<tr>
<td>008004 Passive</td>
<td><img src="image15.png" alt="Image" /></td>
<td><img src="image16.png" alt="Image" /></td>
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<tr>
<td>Double side molding</td>
<td><img src="image17.png" alt="Image" /></td>
<td><img src="image18.png" alt="Image" /></td>
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<tr>
<td>Recessed Substrate</td>
<td><img src="image19.png" alt="Image" /></td>
<td><img src="image20.png" alt="Image" /></td>
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<tr>
<td>Cavity Substrate</td>
<td><img src="image21.png" alt="Image" /></td>
<td><img src="image22.png" alt="Image" /></td>
</tr>
<tr>
<td>Flex Substrate</td>
<td><img src="image23.png" alt="Image" /></td>
<td><img src="image24.png" alt="Image" /></td>
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<tr>
<td>SLIM/SWIFT</td>
<td><img src="image25.png" alt="Image" /></td>
<td><img src="image26.png" alt="Image" /></td>
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<tr>
<td>TSV</td>
<td><img src="image27.png" alt="Image" /></td>
<td><img src="image28.png" alt="Image" /></td>
</tr>
</tbody>
</table>
Si Photonics

- 20um diameter / 40um pitch
- 2~5K bump count (nom)
- Known Good Die
- Both MR & TC available
- Control for alignment
- Various customized design

Cu Pillar Micro Bump
Wafer Level Process/CoW
Chip to Board Connection
Optical Coupling
Technologies for Photonics

Chip on wafer technology

System in Package technology

Cu pillar bump
LAB (Laser Assisted Bonding) Technology for lower stress attach

- **New interconnection solution using laser beam after F/C bonding**
  - Only die heat up with area laser (Local reflow concept)
    - Low thermal stress between PCB and die
  - Fast solder melting : High UPH (Same as mass reflow)

- **Target markets**
  - Mobile, networking, consumer, CPU/GPU
  - BB, AP, logic, ASIC
  - Low K device (28nm, 20nm, 14/16nm)

- **Technology advantage**
  - Cost effective process
  - Lower thermal stress than mass reflow
# Amkor Tester Availability

<table>
<thead>
<tr>
<th>Digital/ Mixed</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
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<tbody>
<tr>
<td>RF</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Analog/ Discrete</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Digital/ Mixed**: Quartet/D10/Catalyst/J750(EX)/IFLEX/V83K/V93K SD&PS, T2000/V93K SmartScale/uFLEX, Catalyst/LTX Fusion, ARMAR(PXI)/V93K PSRF/IFLEX/uFLEX
- **RF**: ETS-88/364/Catalyst/J750/ASLXASL1K/PIXI/Focus Test, ETS-600/800/STATEC
- **Analog/ Discrete**: Magnum PV/SV/SSV/Maverick/J750(EX)/T53XX/T55XX
- **Memory**: Magnum5/Aspen-1/T5503HS
- **CIS**: IP750/T2000ISS

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Amkor Confidential 32
Amkor MEMS Tester Development

- 9DOF (Mag+Accel+Gyro)
- 6DOF (Mag+Accel)
- RF MEMS
- Emerging MEMS
- Optical MEMS
- Temperature
- Humidity
- Pressure
- Gyroscope
- Accelerometer
- uPhone (Top/Bottom)
- E-compass

Overmolded PKG □ Cavity PKG

- < 2013
  - Development Plan
- 2014
  - Development Ongoing
  - Amkor Developed Solution
- 2015
  - Commercial Solution in Amkor production
- 2016
  - H/W in ATP
  - S/W in ATK
Global ECO-Society System