Agenda

- EUV Insertion focus
- EUV Benefits
- Field performance
  - Productivity
  - Imaging, Overlay, Defectivity
- Infrastructure status
- Summary
EUV insertion is focusing on the 7nm node

- EUV insertion is currently focusing on the 7nm node
  - Production 2018, system shipments 2017
  - Insertion will be determined by the production readiness of EUV versus the complexity of multiple patterning

- EUV initially will replace the most difficult multiple patterning layers
  - Other layers will remain allocated to immersion for the foreseeable future

- DUV and EUV will be available in parallel for many years to come
  - ASML remains committed to advancing both technologies to provide the mix that best meets customers’ performance and cost requirements
7nm chip manufactured with EUV system

IBM: “Industry’s first 7nm node test chips with functioning transistors”

- Close to 50 percent area scaling improvements over today’s most advanced technology
- Scaling, materials and process improvements could result in 50 percent power/performance increase for mainframes, servers

Source: IBM press release, 9 July 2015
EUV Industrialization Roadmap supports 7nm insertion
By >1500 wafers per day in 2016

<table>
<thead>
<tr>
<th>Timing</th>
<th>Source power [W]</th>
<th>Throughput [Wafers/hr]</th>
<th>Efficiency* [%]</th>
<th>Productivity [Wafers/day]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>80</td>
<td>&gt;55</td>
<td>&lt;50%</td>
<td>&gt;500</td>
</tr>
<tr>
<td>2015</td>
<td>125</td>
<td>&gt;75</td>
<td>&gt;50%</td>
<td>&gt;1000</td>
</tr>
<tr>
<td>2016</td>
<td>250</td>
<td>&gt;125</td>
<td>&gt;55%</td>
<td>&gt;1500</td>
</tr>
</tbody>
</table>

*Efficiency = system availability x customer utilization x customer rate efficiency
Logic typically 55%, for DRAM 70-75% (>2000 WPD)
Illustrative numbers used for WPD model
EUV reduces complexity and thus cycle time

<table>
<thead>
<tr>
<th>Node</th>
<th># of litho steps</th>
<th># OVL Metrology</th>
<th># max metrology / litho steps</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 nm</td>
<td>8 (Immersion)</td>
<td>9-11</td>
<td>2</td>
</tr>
<tr>
<td>10 nm</td>
<td>23 (Immersion)</td>
<td>36-40</td>
<td>3</td>
</tr>
<tr>
<td>7 nm</td>
<td>33 (Immersion)</td>
<td>59-65</td>
<td>4</td>
</tr>
<tr>
<td>7 nm</td>
<td>9 (EUV)</td>
<td>12</td>
<td>3</td>
</tr>
</tbody>
</table>

Layers:
- 20 nm (Immersion): 8x Masks
- 10 nm (Immersion): 23x Masks
- 7 nm (Immersion): 33x Masks
- 7 nm (EUV): 9x Masks
EUV: Reduced complexity enables faster ramp and higher yield

Source: ASML model
EUV improves circuit performance, yield, design flexibility

Metal Line Wire Resistance distribution improved with EUV

“In this 10nm node demonstration, EUV wafers with single exposure have tighter distribution compared to optimized multi-patterned 193i lithography”

Source: Jeffrey Shearer et al, IBM, AVS, Nov 2014

Hard-to-route design can get up to 36% area improvement with EUV

Source: Lars Liebmann et al, IBM, SPIE, Feb 2015
Moore’s Law cost reduction stays on track with EUV

Multiple patterning costs reduced

NoN = Node on Node
YoY = Year on Year

Source: ASML, IC Knowledge, IMEC
Validated with external consultants
Source power and availability drive wafers/day

**Source power**
- All field systems have minimum 40 Watts
- 80 Watt upgrades completed at multiple customer sites
- Dose-controlled 130 Watts demonstrated at ASML

**Availability**
- 55% availability on average for all NXE:3300B sites
- Several sites achieved average availability of >70% for one week
- One customer has achieved a 4-week average availability of 70%
- Availability upgrades being rolled out

**Productivity**
- Champion data: 1022 wafers/day
- >600 wafers/day achieved on multiple systems, multiple days
- One customer has exposed >500 WpD over 28 consecutive days
EUV power scaling: three levers

- CO$_2$ power
- Conversion efficiency
- EUV energy available for exposure

- Increase CO$_2$ power
- Increase conversion efficiency
- Lower dose overhead

NXE:3100 (“NOMO”)

250 W

NXE:33x0B (“MOPA-Pre-Pulse”)
EUV power above 100W by improved conversion efficiency

High Power Seed System drives up conversion efficiency by higher CO$_2$ peak power

MOPA + Pre-pulse (HPSS) Seed System with 
high power pre-amplification

Drive Laser

3-stage power amplification

Beam Transport & Final Focus

Vessel

with HPSS
130 Watt dose-controlled EUV power shown at ASML

*With high-power CO$_2$ system*
Focus 2015: improving source availability

More than 50 improvement items identified, field upgrades throughout 2015

More than 50 availability improvement items have been identified.

Projects are underway to make these improvements available on customer systems throughout this year.
2015 target >1000 wafers/day proven at 80W
Capability > 1200 wafers per day at maximum utilization shown

Configuration:
- NXE:3300B
- EUV Source:
  - UP2: 80 Watts configuration
  - UP1: 40 Watts configuration
- Customer exposure recipes

Wafers per day (24 hour period)

Customer systems (NXE:3300B)
- UP2
- UP2
- UP1
- UP1
- UP1
- UP1

Maximum number of customer wafer exposures in a 24 hour period
> 500WPD in 4 consecutive weeks proven at customer

Automated reticle & wafer loading. Imaging & overlay in specification

Recent four-week productivity on a NXE3300

- Process conditions
  - Wafers of various lot sizes with required dose, CD, and overlay
- 4-week-averaged WPD: 518 wafers
  - Total wafers processed: 15040
- 4-week-averaged tool availability: 70.2 %

One bar represents a single day
7nm Logic clip imaged with good fidelity

*Routed 2D semi-gridded Metal, 36x38nm (P\textsubscript{V} x P\textsubscript{H})*

This example would require 4 exposures with 193 immersion – or one with 0.33NA EUVL

Conditions: NXE:3300B, annular illumination, 60nm resist, 40mJ/cm\(^2\) dose
NXE:3350B Supports 7nm logic insertion by strongly improved overlay and resolution

- Resolution: 16nm
- Full wafer CDU: ≤ 1.3nm
- DCO: ≤ 1.5nm
- MMO: ≤ 2.5nm
- Focus control: ≤ 70nm
- Productivity: ≥ 125 WPH

Key improvements:
- Reticle Stage: Better thermal control, increased servo bandwidth
- Projection Optics: Higher lens transmission, improved aberrations and distortion
- Off-Axis Illuminator: FlexPupil
- Wafer Stage: Improved thermal control
- New UV level sensor
- Improved air mounts
- Overlay set up: Set-up and modeling improvements
- SMASH sensor: Improved alignment sensor
- Spotless NXE: Automated wafer table cleaning

Imaging/Focus: overlay
Productivity: overlay
NXE:3350 Imaging meets 7nm requirements

16nm dense lines and 20nm iso space: 0.6nm Full Wafer CDU, 0.4nm intra-field

<table>
<thead>
<tr>
<th>Test item</th>
<th>Unit</th>
<th>Spec</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Imaging 16nm dense lines CDU</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intrafield at best focus</td>
<td>nm</td>
<td>≤1.4</td>
<td>0.5</td>
</tr>
<tr>
<td>Intrafield at ±30 nm off focus</td>
<td>nm</td>
<td>≤1.8</td>
<td>0.6</td>
</tr>
<tr>
<td>Full wafer at best focus</td>
<td>nm</td>
<td>≤1.6</td>
<td>0.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test item</th>
<th>Unit</th>
<th>Spec</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Imaging 20nm isolated spaces CDU – H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intrafield at best focus</td>
<td>nm</td>
<td>≤1.1</td>
<td>0.4</td>
</tr>
<tr>
<td>Intrafield at ±30 nm off focus</td>
<td>nm</td>
<td>≤2.5</td>
<td>0.7</td>
</tr>
<tr>
<td>Full wafer at best focus</td>
<td>nm</td>
<td>≤1.3</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Tested with new ATP – 0mm field spacing and 15x9 grid
NXE:3350 Matched Machine Overlay: 2.2nm

Full wafer, matched to Baseline MMO wafers, Wafer Error Correction applied

Lot (2.0,2.2)

99.7% (nm)

Spec. 2.5nm
Front-side reticle defectivity: 10x reduction/year realized

Customer requirement for full production without pellicle

<table>
<thead>
<tr>
<th>Test</th>
<th># Cycles</th>
<th># Added Particles</th>
<th>PRP Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>228</td>
<td>0</td>
<td>&lt; 0.004</td>
</tr>
<tr>
<td>B</td>
<td>140</td>
<td>0</td>
<td>&lt; 0.007</td>
</tr>
<tr>
<td>C</td>
<td>450</td>
<td>0</td>
<td>&lt; 0.002</td>
</tr>
<tr>
<td>D</td>
<td>222</td>
<td>1</td>
<td>0.0045</td>
</tr>
<tr>
<td>E</td>
<td>133</td>
<td>0</td>
<td>&lt; 0.007</td>
</tr>
<tr>
<td>Cumulative</td>
<td>1173</td>
<td>1</td>
<td>0.0008</td>
</tr>
</tbody>
</table>

Added particles > 92nm per reticle pass

- NXE:3100
- NXE:3300B
- NXE:3350B
EUV pellicle films successfully tested in ASML EUV tools
Mechanical compatibility and imaging performance of pellicle film demonstrated

Pellicle film

Pellicle film + frame on reticle

2013

2014

Reticles courtesy of Intel
Removable NXE Pellicle frame concept in development

- CTE matching border to frame
- Remountable fixture to stud interface
- Removable stud to reticle connection
- Flexures prevent reticle deformation
- Optimized frame size
- Frame suspended from reticle
Photoresist approaching 7nm requirements

ADT, NXE:3100, NXE:3300 as measured by ASML/IMEC

CAR: chemically amplified resist

13nm HP resolution with CAR dose to size 31.5 mJ/cm²
LWR < 2.7nm

13nm HP resolution with non-CAR dose to size 35 mJ/cm²
LWR < 2.6nm
EUV mask blank defect density is steadily improving

- EUV blanks with single digit (ML) defect count at 50 nm become commercially available
- Gap to the RM still needs to be closed for HVM
- Advanced inspection capability is required for further defect reduction
EUV Insertion: “WHEN” not “IF”

- Customers differ in exactly “WHEN” EUV will go to volume production
  - EUV insertion is focusing on the 7nm node
  - Production 2018, system shipments 2017

- EUV is making continued progress on the Wafers-per-Day roadmap
  - >500WpD at multiple customers
  - >500WpD over 4 consecutive weeks shown at one customer
  - Roadmap in place to deliver 1500 WpD in 2016 for 7nm insertion
  - Continued focus on availability to >90%

- EUV imaging & overlay meeting 7nm node requirements

- EUV infrastructure progressing towards 7nm volume production