3D-IC Co-Design for Power, Performance and Cost

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It’s not always about process scaling

- **System Requirements**: Bandwidth, Power, functionality, COMPLEXITY
- **Obvious Solution**: Jump to next process node: 20nm/14nm/10nm, BUT
  - NOT really shrinking!! (Analog Circuit? Variability, Leakage? And Utilization%?)
  - Expense of IP re-built and validation! Verification cost? Risk? T2M?
  - **And what about COST?**
  - What about CIS, MEMS, Silicon Photonics, RF, Non-volatile, PMIC → NOT always in a single die!

"We know how to get to smaller size nodes, but we see economic indicators slowing and we are worried about it — we can see the end from here. If we can’t make cheaper transistors, we’ll look to other things like 3D."

Paul Jacobs, CEO, Qualcomm 8/22/13
Short-, medium-, and long-term path to 3D-IC

Si Partitioning with TSV Interposer
- Market: FPGA
- Xilinx in 2010
- 2011-2013

Memory Cube with TSVs
- MARKET: Server and computing
- Micron, Samsung
- 2012-2014

Logic + memory w/ 2.5D TSV Interposer
- MARKET: Server, Telecom, datacom, gaming
- Hi-Silicon
- 2013-2015

Memory + Logic with TSVs
- MARKET: HP mobile/tablet, gaming processors, HPC
- 2015-2016

Heterogeneous Integration w/o TSV
- MARKET: IoT devices, wearable, Automobile
- 2015~

Standards, ecosystem, cost
Review: 2.5D Silicon Interposer for Performance Driven Applications

- Interposer enables high performance/high bandwidth applications through massive interconnects among dies, particularly logic dies and memory dies;
- TSVs in SI Interposer die provide shorter routes for high speed signals, and deliver adequate power/ground connections to both logic and memory dies;
- Metal mesh and MiM Cap in Silicon interposer further enhance the performance through better SI and PI;
- Silicon interposer as better heat conductor for improved thermal dissipation in a small form factor to achieve higher performance.

Silicon Interposer is an additional cost/What about System Level Cost?
3D Stack and/or Monolithic 3D for lower cost

• No additional SI Interposer cost, but TSV and Wafer Thinning

• TSV-Less Integration
  – No wafer thinning, less yield loss
  – Face2face uBump connection for multi-die stack
  – Integrated Fan out WLP

• Monolithic 3D-IC
M3D: could be more about uBump than TSV

How to have physical synthesis that generates 3D-aware netlist?

How to do CTS when it may across multiple dies, with different processes?

How to partition so that the dies are similar in size for WL stacking?

How to do DFT, together, or separately?

What granularity for floor planning, and P&R?

How to sign off for timing across die at MMMC?

3D-IC using fine-pitch uBumps for inter-die P&R Optimization using EDI/Innovus
IoT: SOC, Or Heterogeneous Integration?

- Processor Subsystem
  - Cortex-M
  - RTL Based
  - Library/PMK/SIP/HIP/VIP → Digital Top SOC flow
  - Or

- Low Power Analog
- TxRx/ADC

- Low Power
- Analog
- TxRx
- ADC

- PB/SI
- RF
- Flash

- Sensors
- MEMS
- VR/BM/CG

Implement Cortex-M in VDI and then integrated, verified in existing virtuoso top
IoT: SOC, Or Heterogeneous Integration?

3D-IC in Single Package, without TSV

Lower Cost integration for IoT, automobile etc;
Various FO-WLP Structures

Single-Layer RDL

Multi-Layers RDL

3D Stacked Info on Package Substrate

3D Stacked PoP
Proto-type planning to implementation
Fanout-WLP

Plan
Prototype
Optimize Interconnect
Implement
Refine

Planning Chip-PKG-PCB in single platform-OrbitIO

Physically implementation & refine in SiP
Cross-fabric interoperability for 3D-IC Design

Pre-layout co-simulation (Allegro Sigrity SI Explorer)

OrbitIO interconnect architect (die/interposer/package/board)

Innovus & Virtuoso solutions

SIP

Silicon Refinement flow

Package Refinement flow

Signoff co-simulation (Sigrity solution)

Allegro PCB solution

Optimization

Refinement
New Challenges in Fab-like WLP Designs

- Traditional package design tools such as Allegro are based on PCB and IC PKG manufacturing rules; for substrate layout the tools do not understand IC manufacturing rules, IC routing rules, or IC-specific structural rules.

- IC level Physical verification integrated in package design tool such as stringent metal density rules, etc.

- GDS2 Stream in and out in package design tool

- DRC error fix directly inside package design tool

- Electrical and thermal co-analysis
Example: Package designs for SC Verification

- Vectorization
3D-IC: Package bump co-optimization flow

Before bump optimization

After bump optimization

EDI/Virtuoso

Die abstract of logic die

Import die abstract (Distributed co-design)

Add package component

Connectivity optimization

Routing feasibility

Package model extraction
For SI/PI analysis
Electrical Performance and Analysis Requirement for INFO-WLP

- High Q inductors and self-resonance frequency to enhance electrical performance
  - Embedded passive component modeling \(\rightarrow\) 3DEM Fullwave

- Lower power consumption in RF circuit applications
  - Power and ground RLC model extraction and IR drop analysis \(\rightarrow\) Package model extraction and chip-package co-simulation

- Better SI-eye-diagram improvement
  \(\rightarrow\) High density routing on post-passivation interconnects (PPI)
  - Crosstalk hot spot analysis
  - System level bus analysis
Multi-Dies-package-board thermal co-simulation
Thermal Throttle is #1 limiter now

- Sigrity PowerDC computes Temperature map including multiple dies, package and board
- Voltus computes temperature dependent Power map of each die (leakage, dynamic)
- Iterate co-simulation until results converge (equilibrium, transit)
Integrated “Voltus + Sigrity” solutions for IC-centric chip-PKG co-analysis

- Independent installation
- External file exchange
- Neither IC- nor system-centric
- Not user-friendly flow
  - PKG setup challenges for IC designer
  - PKG model connection in MCP

Current Flow

Integrated Flow

Oct. 2015

- Embedding Sigrity™ technology in Voltus™ solution
  - XtractIM™ and PowerDC™ technologies
  - Independent Sigrity installation
- File exchange transparent to user
- Voltus cockpit calls Sigrity solution
- Visualization
- Post-Oct plan - thermal
3D-IC Solutions with flexible Implementation Cockpits

**SOC entry point**
- Virtuoso
- PVS
- Quantus
- Sigrity
- Allegro Sip
- Tempus
- Voltus
- ET*
- Genus
- PowerDC
- Wide IO/H BM

**Virtuoso entry point**
- Virtuoso
- PVS
- Spectre
- Tempus
- ET*
- Wide IO/H BM
- Genus
- PowerDC
- Voltus
- XPS
- Quantus

**System entry point**
- Allegro SiP/OrbitIO
- Tempus
- ET*
- PowerDC
- Voltus
- Genus
- Quantus
- XPS
- PVS
- Wide IO/H BM
Summary

• Different 3D-IC integration technologies are needed for high performance centric, or low cost applications;
• All 3D-IC integration technologies, whether high performance, or lower cost, will reduce system power consumption;
• Mobile, IoT, Wearable in consumer applications will drive the TSV-less 3D integration technologies such as fanout WLP to mass production;
• Monolithic 3D integration will both bring even higher performance and lower power in smaller form factor in the future;
• Implementation method varies for different 3D integration technologies, but an integrated co-design environment and electrical and thermal co-analysis is a must.
3D-IC signoff and electrical analysis

- **Tempus™ tool**
  - Die-to-die timing report

- **PVS**
  - Layer identification
  - Easy-to-use debugging environment for users to troubleshoot 3D-IC design graphically
  - Integrate with Cadence EDI P&R tool to support die stack configuration

- **Sigrity tool**
  - XcitePI™ die interconnect extraction including TSVs
  - On-die electrical performance assessment results
  - Multi-die and package SSN co-simulation results
Interposer and package Implementation in SiP
Logic, memory, interposer C4 bump and Ball

Si-Interposer

C4-bump large octagon
u-bump small octagon

BGA Ball

Logic
MEM
Interposer
PKG

“>config substrate layers”

Package substrate
SiP centric flow

- Design Import & Creation
- Net Mapping & Optimization
- Route Feasibility
- Import OrbitIO to SiP Layout
- Package Implementation
- Breakout & Full Routing (AiBT & APR)
- Simulation

OrbitIO™ interconnect architect

SiP Layout

Sigrity™ solution
Separate Databases
One Database
Add Interposer to Package
Add other dies on interposer

- Optimize net connectivity from ball to dies through interposer
- Route interposer
  - Break-out components
  - Route using AiXT functions, Spectra or APR
- Export interposer routes as GDSII
**THERMAL - WIDE IO VS POP**

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- 4" smartphone mechanics, typical chipset
- Application of 10W SOC perf peak starting from 2W SOC steady state

**Observation:** POP thermal performance better than WideI0
- TSV requires silicon die to be reduced to 50-70um, which results in poor lateral heat distribution
- Thermally tightly coupled WideI0 DRAM heats up much faster than in POP
- WideI0 DRAM performance reduced at Tj > 85°C due to increased refresh cycle requirements

*Source: ST-Ericson*